A 100–117 GHz W-Band CMOS Power Amplifier With On-Chip Adaptive Biasing

Zhiwei Xu, *Senior Member, IEEE*, Qun Jane Gu, *Member, IEEE*, and Mau-Chung Frank Chang, *Fellow, IEEE*

***Abstract*—A W-band power amplifier (PA) has been realized in 65 nm bulk CMOS technology, which covers 100 to 117 GHz. It delivers up to 13.8 dBm saturated output power with up to 15 dB power gain and 10% PAE, which also achieves better than 10.1 dBm output P1 dB. The PA features compact realization with transformer-coupled three stages and on-chip input/output baluns to facilitate single-ended characterization. To ensure stability and boost efficiency, it adopts cascode structure in the first two stages and common source amplifier in the last stage. To improve the PAE and linearity, an adaptive biasing circuitry is incorporated inside the PA. The entire PA core occupies 0.041 mm^2 die area and burns about 180 mW with the adaptive bias circuit consuming only 0.002 mm^2 active chip area.**

***Index Terms*—Adaptive biasing, CMOS, output $\mathrm{P}_{1\,\mathrm{dB}}$, PAE, power amplifier (PA), W-band.**

I. Introduction

MILLIMETER wave (mm-Wave) communications started to attract interest in recent years due to their abundant spectra for high speed wireless data communications. It also empowers radar and imaging applications due to its unique capability to penetrate fog/dust and detect concealed objects. Different from its low frequency RF counterparts, mm-Wave wireless communication systems tend to use beam forming techniques to increase antenna directivity so as to boost gain and alleviate the tight communication link budget at the cost of more sophisticated systems, which mandate multiple signal paths with different phases to form desired transmission beam. Multi-path systems entail on-chip PAs to avoid complicated assembly at high frequencies. On the other hand, the System-on-a-Chip (SoC), manifested by the single chip Bluetooth radio and integrated 802.11 wireless local area network (WLAN) chip, becomes the standard in portable devices with low bill–of–materials (BOM) and also validates CMOS capability for single chip radio. With fast transistors from continuous scaling deep-submicron CMOS, it is expected that the mm-Wave phase array transceivers can be realized in CMOS as well. Among all the blocks, the CMOS power amplifier is one of the most challenging blocks to fulfill this quest.

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Z. Xu is with HRL Laboratories, LLC, Malibu, CA, 90265 USA (e-mail: zaxu@hrl.com).

Q. J. Gu is with the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611 USA (e-mail: qgu@ece.ufl.edu).

M.-C. F. Chang is with the Department of Electrical Engineering, University of California at Los Angeles, Los Angeles, CA 90095 USA.

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II. CMOS and Cascode Configuration

Although deep-submicron CMOS technology enables the mm-Wave transceiver development [3] with its high $\mathrm{f_T}$ and $\mathrm{f_{MAX}}$ devices, it still poses significant challenges to high performance power amplifier design due to the shrinking supply and low device breakdown voltages. It constrains PA output power ($\mathrm{P_{out}}$), linearity, power-added efficiency (PAE), gain, stability, and reliability. Low frequency PA can use long channel I/O devices, whose speed is high enough to mitigate these problems. However, such scheme could not work in mm-Wave frequency range. Lots of research has been devoted to mm-Wave CMOS PA developments for V-band links [1]–[5]. [6] presented a W-band CMOS PA with 6.6 dBm saturated output power and 8.5 dB gain. Various techniques have also been explored to improve PA linearity. [7] proposed $\mathrm{g_m}$-linearization to achieve the required linearity for 2.4 GHz WLAN by separating the amplification devices into main device biased at class-A region and auxiliary device biased at class-B region to realize a linear effective $\mathrm{g_m}$ over a wide dynamic range. This scheme is not very efficient in mm-Wave regime because class-B bias lowers the device speed. Nonlinear capacitance compensation technique has also been investigated and applied for the PA up to 8.8 GHz [8]. It, however, induces extra capacitance load and hinders its employment in high frequency regime.

In this PA, we adopt cascode architecture for the preamplifier to enhance the gain and reverse isolation, which ensures stability. And we connect the cascode deep N-well devices' bulk to a high voltage (0.6 V~1 V), which allows a higher supply voltage for larger output power and better linearity without reliability concern. In the last power delivery stage, a common source amplifier configuration is used to offer high efficiency, where a separate supply voltage is applied. This hybrid architecture, comprised of both cascode and common source amplifiers, demonstrates excellent performance with a slight PAE degradation from the preamplifiers. The simulated K factor is larger than 1 across the entire spectrum, that validates the PA stability.

III. W-Band Power Amplifier Design

Fig. 1 presents the W-band power amplifier schematic. It features transformer-coupled three-staged differential architecture with integrated input and output baluns that convert the off-chip single-ended signal into on-chip differential signals and also serve as 50 Ω matching networks simultaneously. The input balun and inter-stage transformers have around 1:1.5 transformation ratio, and the output balun has 1:2 transformation ratio. The simulated coupling coefficients are in the range of 0.7 to 0.8. To improve simulation accuracy, each device's interconnections

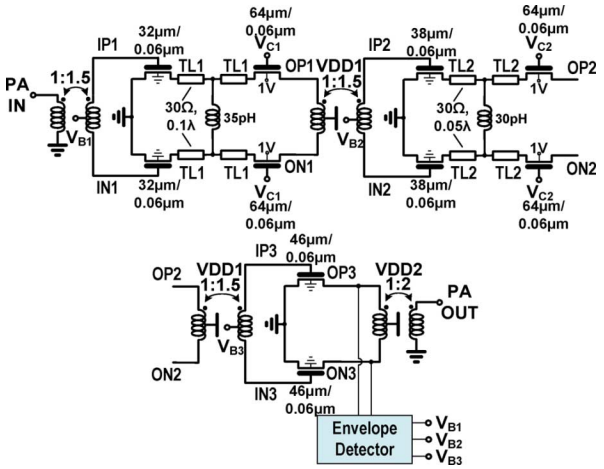

Fig. 1. W-band power amplifier with adaptive biasing.

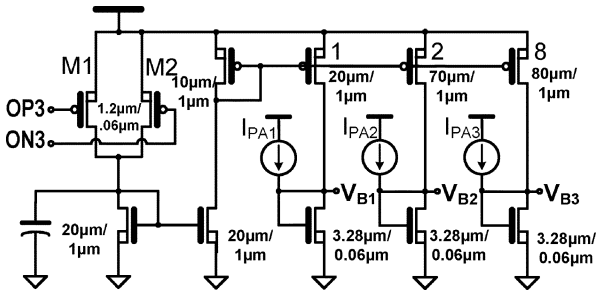

Fig. 2. Adaptive biasing scheme by using envelope detector.

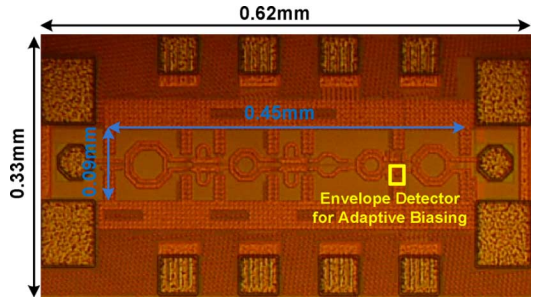

Fig. 3. Amplifier die photo.

have been simulated by EM tools, such as ADS Momentum, and included in the design.

Each PA stage is biased at class-A type. The first two stages provide most of the voltage gain and have 2 dB higher voltage compression point than that of the output stage based on simulations. To ensure linearity performance across the entire dynamic range, a large dc bias current is needed during high output power period. However, it is not power efficient to maintain the high bias current during low output power period. Normally, the system only works at its peak output power in less than 10% period, which implies the PA would waste significant power if maintaining a high dc bias current. To improve PAE and assure PA linear operation across its dynamic range simultaneously, an adaptive biasing scheme is adopted by tracking the PA output power and adjusting each PA stage bias current accordingly. Fig. 2 sketches the PA adaptive biasing circuitry. Two PMOS transistors, M1 and M2, serve as envelope detector to extract the PA output amplitude before the output balun and convert it into bias current. Then each stage current mirror copies the current in a dedicated ratio and superposes onto each PA stage bias current.

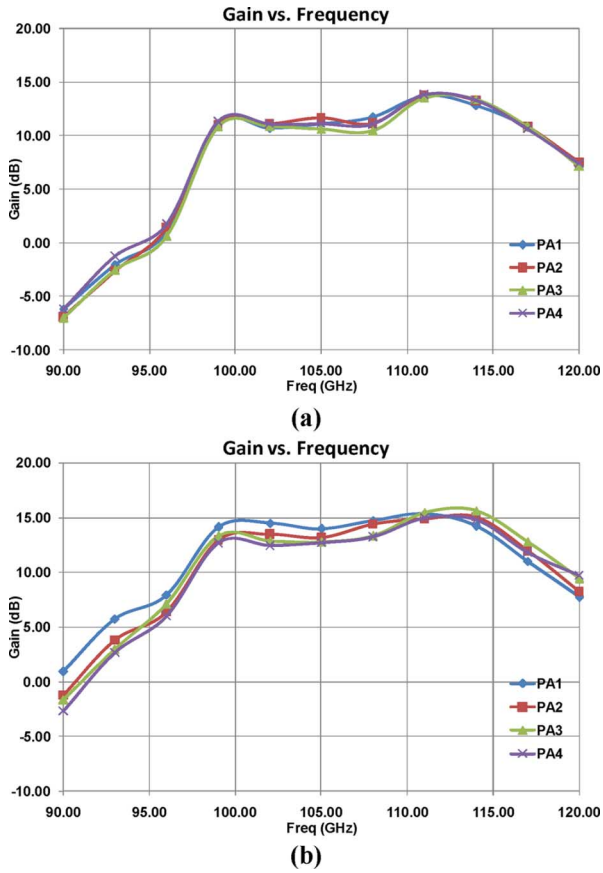

Fig. 4. Measured W-band PA gain under (a) $\mathrm{VDD1} = 1.4\ \mathrm{V}, \mathrm{VDD2} = 1\ \mathrm{V}$ (b) $\mathrm{VDD1} = 2\ \mathrm{V}, \mathrm{VDD2} = 1.2\ \mathrm{V}$.

When PA transmits a low output power, the output amplitude is small, so as the generated current. Thus the major bias current for each PA stage are $\mathrm{I_{PA1}}$, $\mathrm{I_{PA2}}$, and $\mathrm{I_{PA3}}$, respectively. When the PA output power is large, it triggers the envelope detector and generates currents that are mirrored as the extra bias current accordingly to sponsor the PA large output swing and boost its linearity. The current mirror factors are optimized to ensure the PA linearity across the output dynamic range and maximize its PAE as well. Such scheme introduces negligible degradation on the main PA performance due to the small capacitance of the transistors M1 and M2. However, it does introduce a feedback loop within the PA, whose bandwidth is preferred to be wide to maximize the PAE improvement. A bandwidth of about 50 MHz is adopted in this design.

IV. Measurement Results

The PA has been fabricated in TSMC 65 nm bulk CMOS. Fig. 3 shows the PA chip micrograph, which occupies $0.62 \times 0.33\ \mathrm{mm}^2$ and $0.45 \times 0.09\ \mathrm{mm}^2$ with and without pads respectively. The adaptive biasing circuit consumes less than $0.002\ \mathrm{mm}^2$ chip area and resides in the PA output stage before the balun.

Harmonic mixer is used to sweep the power amplifier gain, then a power sensor is used to characterize the amplifier output power, linearity and power added efficiency. The power source consists of a W-band power source by Virginia Diode Inc. (VDI) and a tunable attenuator with 50 dB dynamic range. To accurately characterize the PA at W band is not trivial due to

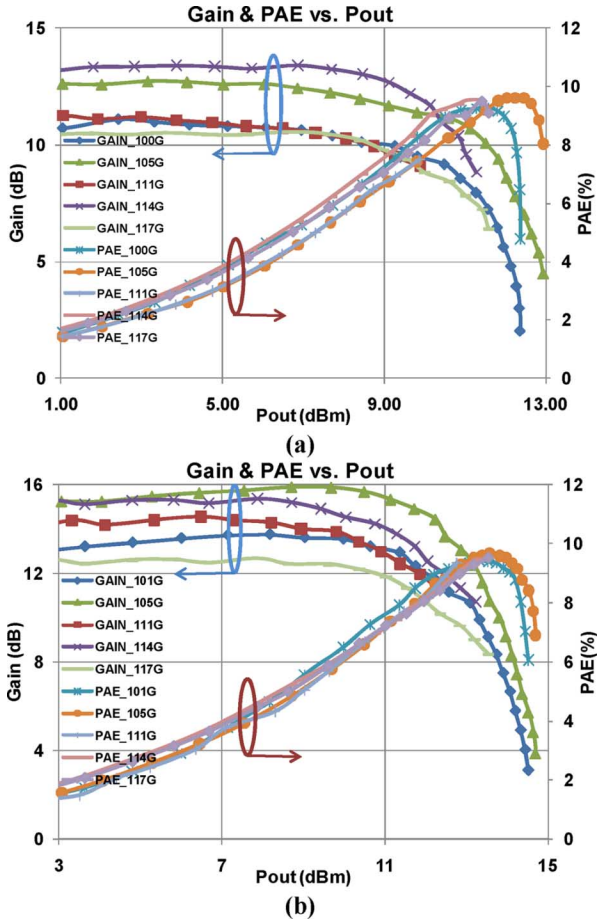

Fig. 5. Measured W-band PA gain and PAE versus Pout at 100, 105, 111, 114, and 117 GHz under (a) $\mathrm{VDD1} = 1.4\ \mathrm{V}$, $\mathrm{VDD2} = 1\ \mathrm{V}$ (b) $\mathrm{VDD1} = 2\ \mathrm{V}$, $\mathrm{VDD2} = 1.2\ \mathrm{V}$.

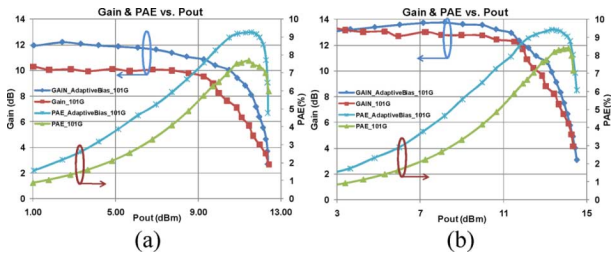

Fig. 6. Measured gain and PAE versus Pout comparison between PAs wi/wo adaptive biasing at 100 GHz under (a) $\mathrm{VDD1} = 1.4\ \mathrm{V}$, $\mathrm{VDD2} = 1\ \mathrm{V}$ (b) $\mathrm{VDD1} = 2\ \mathrm{V}$, $\mathrm{VDD2} = 1.2\ \mathrm{V}$.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

PA technology	Working Frequency	Gain (dB)	Psat (dBm)	Peak PAE (%)	P1dB (dBm)	Core Area(mm2)
This work (VDD1=1.4V,VDD2=1V)	100-117GHz	10.3	11.8	**10**	**10.1**	0.041
This work (VDD1=2V,VDD2=1.2V)	100-117GHz	13.4	13.8	**9.4**	**11.2**	0.041
PA wo Adaptive Biasing(VDD1=1.4V,VDD2=1V)	100-117GHz	10.1	12	8.9	9	0.041
PA wo Adaptive Biasing(VDD1=1.4V,VDD2=1V)	100-117GHz	13	13.9	8.5	10.4	0.041
[1] 90nm CMOS	48-65GHz	7	12.3	8.8	9	0.25 (wi PAD)
[2] 65nm CMOS	57-64GHz	15.8	11.5	11	2.5	0.053
[6] 65nm CMOS	75-95GHz	8.5	6.6	N/A	2.2	N/A

non-constant source power and setup loss variations across frequencies. Therefore, a standard through line is used during characterization for de-embedding. Fig. 4 presents the power amplifier gain versus input signal frequency measured from four different dies by a harmonic mixer under two different power supply conditions: low supplies with pre-amplifier $\mathrm{VDD1} = 1.4\ \mathrm{V}$ and last stage $\mathrm{VDD2} = 1\ \mathrm{V}$; high supplies with pre-amplifier $\mathrm{VDD1} = 2\ \mathrm{V}$ and last stage $\mathrm{VDD2} = 1.2\ \mathrm{V}$. Compared with the low supply condition, the PA provides average 2.5 dB more gain under the high supply condition. Compared with simulation, the measurement shows 3 dB lower gain, which could be introduced by the magnetic coupling effect between stages that we didn't incorporate during simulation.

Fig. 5 shows the measured power amplifier gain and PAE versus output power under the identical two different supply conditions. The peak PAE in the low supply condition is about 10% with 11.8 dBm saturated output power, and the peak PAE in the high supply condition is 9.4% with 13.8 dBm saturated output power. At peak PAE, the PA draws 58 mA/40 mA and 64 mA/46.5 mA for the pre-amp stage and output stage under the low supply and high supply conditions, respectively. Fig. 6 shows the measured gain and PAE comparison between PAs with and without adaptive biasing at 100 GHz. The adaptive biasing improves the PAE by about 1.2% in the middle output power regime, which demonstrates about 30% improvement of PAE from 3.1% up to 4.3%. The measurement results at all other frequencies also demonstrate such PAE improvement. Table I summarizes this PA performance and compares it with prior arts. This PA delivers the largest output power with 10% PAE beyond 100 GHz in CMOS.

V. CONCLUSION

A 100–117 GHz W-band CMOS PA with adaptive biasing has been demonstrated in 65 nm CMOS. It achieves 13.8 dBm saturated output power with 10% PAE and larger than 10 dB power gain across the frequency band. It pushes the technology frontier and paves the way for future integrated mm-Wave wireless communications and active radar/imaging applications in CMOS technology.

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