100 GHz integrated CMOS passive imager with >100 MV/W responsivity, $23fW/\sqrt{Hz}$ NEP

Q.J. Gu, Z. Xu, H.-Y. Jian, A. Tang, M.-C.F. Chang, C.-Y. Huang and C.-C. Nien

Presented is a 100 GHz fully differential CMOS passive imager for system-on-chip integration, which features high gain, high sensitivity and high resilience to flicker noise and gain variation. It integrates a low-noise amplifier, a Dicke switch, a detector and a baseband programmable gain amplifier in a single chip, and achieves the best noise equivalent power (NEP) ($23fW/\sqrt{Hz}$/$26fW/\sqrt{Hz}$ for without/with Dicke switch) in CMOS, the highest responsivity (>100 MV/W) in silicon. It also demonstrates 1.96 K noise-equivalent temperature difference in 30 ms integration time.

Introduction: Sub-millimetre-wave imaging is attracting increasing attention owing to its unique capability to penetrate through concealed obstacles such as fabric/fog/dust compared with that of infrared optics. Among them, passive imaging is of particular interest to construct pictures through detecting black body radiation without any emission. However, a frail black body radiation signal demands ultra-high sensitivity and excellent noise-equivalent temperature difference (NETD) with fast response time. In this Letter, we present a 100 GHz fully differential passive imaging receiver with $23fW/\sqrt{Hz}$ noise equivalent power (NEP). The proposed architecture mitigates common mode noise coupling from supplies and substrate, signal quality deterioration due to flicker noise and gain variation to achieve the best imager sensitivity.

Architecture and circuit design: Fig. 1*a* shows the proposed passive imaging SoC architecture. Different from previous approaches [1, 2], applying an analogue integrator before the ADC, this architecture places the integrator in the digital domain to remove its flicker noise. Therefore, all the circuit flicker noise, including the ADC's, can be sampled and cancelled through the digital multiplier and integrator, which is critical to a CMOS passive imager. This work integrates a low-noise amplifier (LNA), a Dicke switch, a detector and a baseband programmable gain amplifier (PGA); an ADC, digital multiplier and integrator are to be integrated in the future. Prior arts [1–3] are all based upon single-ended implementation, which renders the system vulnerable to coupling and noise interferences, especially when integrated with other mixed-signal and digital circuits. For example, the power switching noise would directly couple into the LNA and detector through shared supply or substrate and then overwhelm the weak input signal. On the other hand, a fully differential architecture is more resilient to such noises, therefore is preferred. Simulation verifies that differential implementation can boost the supply rejection ratio by more than 30 dB and also improve system dynamic range.

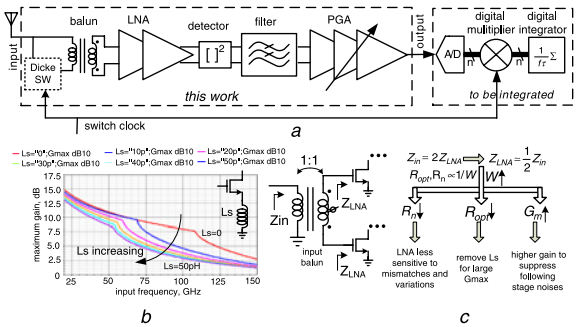

Fig. 1 *Passive imaging architecture to mitigate CMOS flicker noise through digital multiplier and integrator (Fig. 1a); G_{max} of different source degeneration inductor L_S confirms optimum approach without L_S (Fig. 1b); 1:1 balun turns ratio utilised to achieve both minimum noise and maximum gain (Fig. 1c)*

The LNA is the most critical block to achieve an ultra-sensitive CMOS passive imager. Owing to the small receiving power, the noise figure becomes the discriminating spec to the differential LNA, where its minimum noise factor (F_{min}) is independent of device size and can be optimised by setting proper input device current density [4]. The actual LNA noise factor can be formulated as

$$F = F_{min} + \frac{[(G_S - G_{opt})^2 + (B_S - B_{opt})^2]R_n}{G_S} \quad (1)$$

where $Y_S = G_S + jB_S$ and $Y_{opt} = G_{opt} + jB_{opt}$ are source admittance and optimum source admittance, respectively. Both R_n (receiver equivalent noise resistance) and $R_{opt} = 1/G_{opt}$ and are inversely proportional to active device size [4]. Therefore, a wider LNA input device is preferred for three reasons: first, smaller R_n results in a less sensitive noise factor F to process variations and mismatches implied by (1); secondly, smaller R_{opt} avoids source degeneration inductor L_S to degrade the power gain, which is otherwise needed for 50 Ω matching. Fig. 1*b* shows the simulated maximum available gain G_{max} against frequency for different L_S values. It validates that the highest G_{max} can be achieved by removing L_S; thirdly, a larger device provides higher gain to suppress the following stage noises. However, maximum active device size is constrained by the desired operation frequency and practical on-chip passive device options. Therefore, compared with a 2:1 balun turn ratio, a 1:1 ratio is chosen to allow a larger LNA input device and smaller R_n. So the LNA input impedance Z_{LNA} is set at about half of the source impedance Z_{in} at 1:1 ratio, as shown in Fig. 1*c*. Also, a 1:1 turn ratio simplifies the balun design to achieve low loss and good symmetry for better performance compared with other turn ratios.

A Dicke switch is integrated to calibrate circuit internal noise and gain variations. To calibrate all the noises, the switch must be placed in the front of the LNA which imposes stringent requirements on the insertion loss. Fig. 2*a* shows the proposed switch circuit and the corresponding signal detection and reference calibration paths controlled by the switch clock. Because this proposed switch does not expose any active device in the signal path, it not only minimises insertion loss, but also eliminates extra parasitics, which is especially suitable for high frequency operation. As indicated by Fig. 2*b*, the simulated insertion loss is improved from 4.3 to 1.7 dB at 110 GHz and from 8.5 to 1 dB at 220 GHz. Most importantly, improvement increases with operating frequency. As a result, this proposed switch structure is beneficial to ultra-high frequency operations and demonstrates the best performance among reported silicon switches beyond 60 GHz [5].

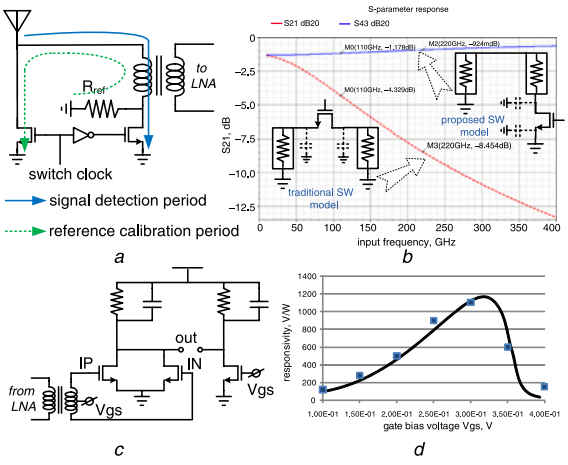

Fig. 2 *Proposed integrated Dicke switch structure and paths during signal detection period and reference calibration period (Fig. 2a); simulated insertion losses of proposed and traditional switch (Fig. 2b); square law detector (Fig. 2c); measured (dot) and simulated (line) responsivities against bias voltage (Fig. 2d)*

The detector extracts the rms power information from the input signal and completes the high frequency operation in the passive imager. However, the low conductance of the CMOS device, compared to its counterpart in bipolar and III-V technologies, often renders the receiver to have poor responsivity, which needs designs to compensate. It can be proved that the NMOS detector, shown in Fig. 2*c*, achieves best performance when biased at the edge of the saturation region and provides the maximum rectification gain, which ultimately leads to the highest detector responsivity. Analysis based on a short channel MOS model [6] predicts detector responsivity, which can be characterised as the second-order derivative of drain current against gate source voltage change, is proportional to the bias current in the subthreshold region, as evidenced by (2). It also implies responsivity can increase with

gate source voltage. However, in the saturation region, the detector responsivity becomes inversely related to bias voltage, indicated by (3). Thus, the highest responsivity may be achieved at the subthreshold/saturation transition region. Fig. 2*d* further validates this by both measured and simulated detector responsivity against gate bias voltage, which agrees with the above analysis.

$$\frac{\partial^2 I_{lin}}{\partial V_{gs}^2} = \mu_0 C_d \frac{W}{L} V_T \frac{1}{\xi} \exp\left(\frac{v_{gs} - V_{TH}}{\xi V_T}\right) \frac{1}{\xi V_T} = \mu_0 C_d \frac{W}{L} \frac{1}{\xi^2} \exp\left(\frac{v_{gs} - V_{TH}}{\xi V_T}\right) = \frac{1}{\xi^2} \frac{I_{lin}}{V_T^2} \tag{2}$$

$$\frac{\partial^2 I_{sat}}{\partial V_{gs}^2} = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} \frac{2}{(1 + (\mu_0/2 v_{sat} L + \theta)(V_{gs} - V_{TH}))^3} \tag{3}$$

In the sub-millimetre-wave passive imager, the signal out of the detector is still quite small. It necessitates a PGA after the detector to boost further the signal strength to the full scale of the following ADC. The PGA features four-stage amplification that adopts Cherry-Hooper architecture, similar as [7], and realises over 20 dB gain with only 4 mA power consumption.

Measurement results: This integrated 100 GHz passive imager has been designed and fabricated in 65 nm CMOS. Fig. 3*a* provides the measured waveform when applied with an external signal source and the Dicke switch clock. The output is a square-wave-like signal running at 1 MHz, which is set by the switch clock frequency. The output high/low DC levels correspond to detection/calibration cycles, respectively. As input signal power increases, the output high DC level increases initially, then reaches the highest level due to saturation; and finally the output low DC level, corresponding to the reference calibration cycle, starts increasing until saturating to the identical highest DC level. This is because the implemented Dicke switch could not completely isolate the external input during the reference calibration cycle. Thus, the output waveform amplitude increases initially with stronger input then decreases due to circuit saturation. The imager responsivity is measured when the Dicke switch is either enabled or disabled. The measured peak responsivity with an enabled/disabled switch are 1.6 and 1.8 MV/W, respectively, which is increased to >100 MV/W with the on-chip PGA that has over 20 dB gain. Output noise voltages are measured at 1 MHz offset without the Dicke switch and at 1.5 MHz offset with the Dicke switch clocking at 1 MHz. NEPs of $26fW/\sqrt{Hz}$ and $23fW/\sqrt{Hz}$ are also demonstrated with the enabled/disabled Dicke switch. It confirms the insignificant performance degradation caused by the proposed Dicke switch. The NETD for 30 ms response time is less than 2 K with the integrated Dicke switch.

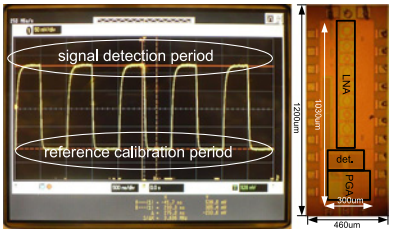

Fig. 3 *Receiver output with integrated Dicke switch, and die photo*
a Receiver output with integrated Dicke switch
b Die photo

In summary, we have demonstrated a fully differential passive 100GHz imager with the best NEP and highest responsivity in CMOS to satisfy the stringent passive imaging requirements (previous record responsivity reported by [2] was 43 MV/W). Fig. 3*b* is the chip photo, which occupies 1.2 × 0.46 mm chip area with pads. The overall power consumption is 62 mW.

Acknowledgment: The authors thank TSMC for foundry support.

22 January 2011
doi: 10.1049/el.2011.0213
One or more of the Figures in this Letter are available in colour online.

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