17.10 A 10b Resistor-Resistor-String DAC with Current Compensation for Compact LCD Driver ICs

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Achieving a higher color depth for LCD drivers requires a higher DAC resolution and a larger circuit die area. Due to the stringent requirement on uniformity, a resistor-string DAC (RDAC) is predominantly used for LCD column drivers. However, the area of the RDAC and related routing lines are prohibitively large for a high-resolution data converter, making it impractical for column-driver ICs in high color depth displays [1].

To avoid the above-mentioned issue, the following DAC architectures were proposed in the past: a CDAC [2], an embedded DAC [3], DACs with current modulation/interpolation [4-5], and a resistor-resistor-string DAC (RRDAC) without unity-gain buffers [1]. However, the CDAC architecture suffers from a long D/A conversion time. The embedded DAC architecture requires a large number of input transistors with long widths and lengths for accurate matching. This results in a large area overhead for high bit interpolation. The DACs with current modulation/interpolation were implemented in 0.1μm CMOS technology, which requires many current switches for modulation/interpolation. If the DACs with current modulation/interpolation were implemented in a low-cost CMOS technology (wider channel length) or a high-voltage technology, they would occupy large die area.

A typical RRDAC, which contains two RDACs and two intermediate unity-gain buffers, may reduce the chip area. The unity-gain buffers can isolate these two RDACs. The buffers, however, have offset errors that can be further spread to the LCD driver output. Consequently, obtaining output uniformity for a high-color depth column driver is rather difficult. Furthermore, each output channel demands two additional buffers with increased power consumption. To reduce the area, researchers have used a RRDAC without unity-gain buffers [1]. Under such condition, parallel channel resistor strings have been connected directly to the global resistor string. This, in fact, affects the reference voltages of the global resistor string.

To overcome these issues, we introduce a type of 10b RRDAC with a current compensation scheme to provide good linearity and uniform channel performance, and simultaneously maintain the 10b DAC at a size smaller than that of a conventional 8b RDAC. A cascode class-AB control is devised to bias the output stage of the output buffer.

Figure 17.10.1 shows the 10b RRDAC by combining a 6b RDAC and a 4b RDAC without the need of unity-gain buffer to isolate parallel-connected resistor strings, yet with current compensation to offset the loading effect. In a column-driver chip, a 6b global resistor string ($64R_1$) is used. Each output channel has a 6b decoder, a 4b channel resistor string ($16R_2$), a 4b decoder, and an output buffer. Based on the higher 6b data signal, the 6b decoder selects two neighboring voltages (V_H and V_L) and connects them to the 4b channel resistor string. For the lower 4b data signal, the 4b channel resistor string divides the output voltage into 16 levels between V_H and V_L. The 4b decoder further selects a voltage from the channel resistor string and propagates it to the output buffer. The current flowing in the channel resistor string is $(V_H - V_L)/16R_2$. To minimize the loading effect, we can then inject currents of $(V_H - V_L)/16R_2$ into both the top and the bottom ends of the channel resistor at the same time. As a result, insignificant static current would flow between the global and channel resistor strings. The reference voltages for the global resistor string therefore remain intact.

All channel compensation currents for a column driver are mirrored from a global compensation current source to minimize the overhead area and power consumption. As shown in Fig. 17.10.2, the global compensation current source senses the voltage difference between two nodes at the middle of the global resistor string and generates the proper compensation current accordingly. Since the sensed voltage difference is $n \cdot (V_H - V_L)$ and the total value of the resistor string in the global compensation current source is n times that in the channel resistor string, the generated compensation current will be set at

$$I_{comp} = \frac{n \cdot (V_H - V_L)}{n \cdot 16R_2} = \frac{V_H - V_L}{16R_2}.$$

Figure 17.10.3 shows the schematic of the output buffer, where the cascode class-AB control, M11-M18, precisely controls the quiescent current of the output transistors. This makes the quiescent current insensitive to the supply voltage.

Using 0.35μm/0.5μm CMOS technology, an 18-channel prototype is fabricated for validating the 10b RRDAC's performance. The test pattern is applied simultaneously to all channel inputs. Figure 17.10.4 shows the measured results in terms of a linear 10b gray scale for RGB-separate gamma on five different chips. The maximum DNL and INL are measured as 0.14 LSB and 0.61 LSB, respectively, with 1LSB = 4.4mV. The DVO is also measured according to 1024 gray scales on five chips. Without applying any off-chip trimming, the maximum inter-chip DVO is 16mV. Figure 17.10.5 shows measured output waveform with a 30kΩ-resistance and 30pF-capacitance load, as the digital data change from "0000000000" to "1111111111". The time to settle within 0.2% of the final voltage is 4μs. Figure 17.10.6 summarizes the performance of the 10b RRDAC compared with the state-of-the-art. Figure 17.10.7 shows the area of the DAC compared with that of a conventional 8b RDAC. The 10b RRDAC occupies 70% of the conventional 8b RDAC area. Figure 17.10.7 also shows the die micrograph with sizes of 530×504μm^2 and 150×504μm^2 for 18 RRDACs and 18 buffers, respectively. The measured results show that the RRDAC with current compensation scheme is very suitable for both small- and large-size LCD applications.

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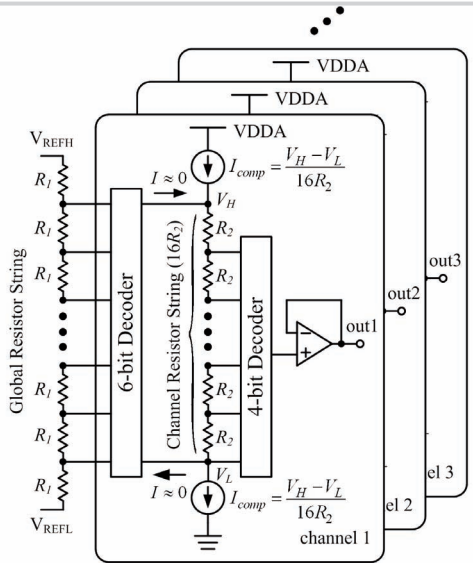

Figure 17.10.1: Architecture of 10b RRDAC.

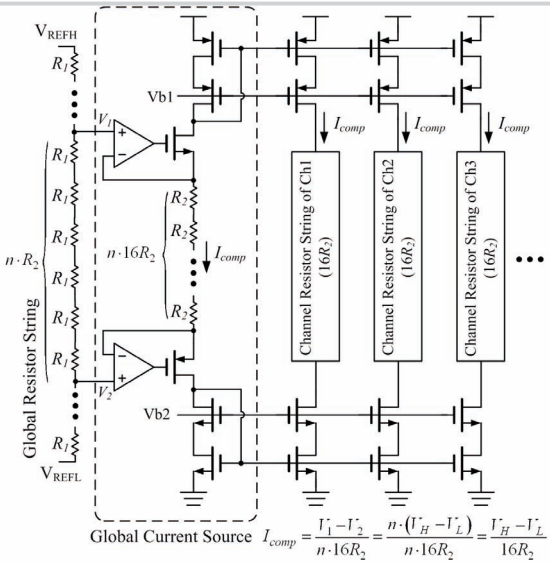

Figure 17.10.2: Schematic of the global compensation current source.

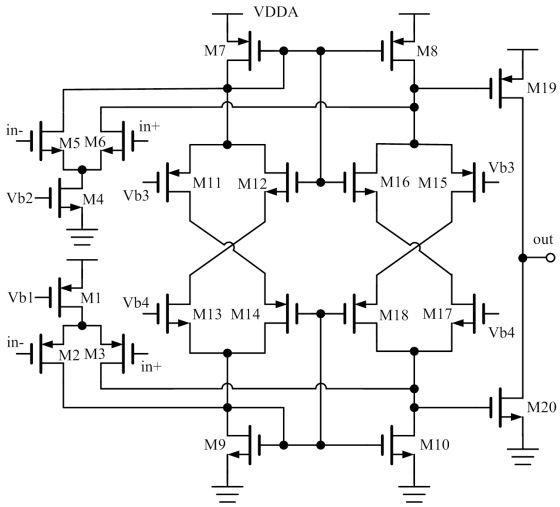

Figure 17.10.3: Schematic of output buffer.

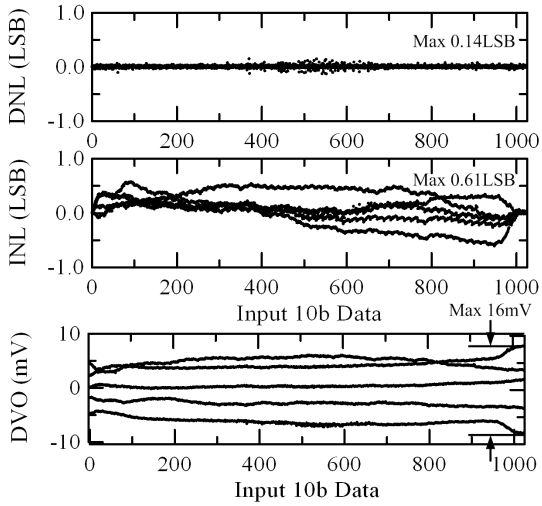

Figure 17.10.4: Measured DNL/INL and DVO from five different chips.

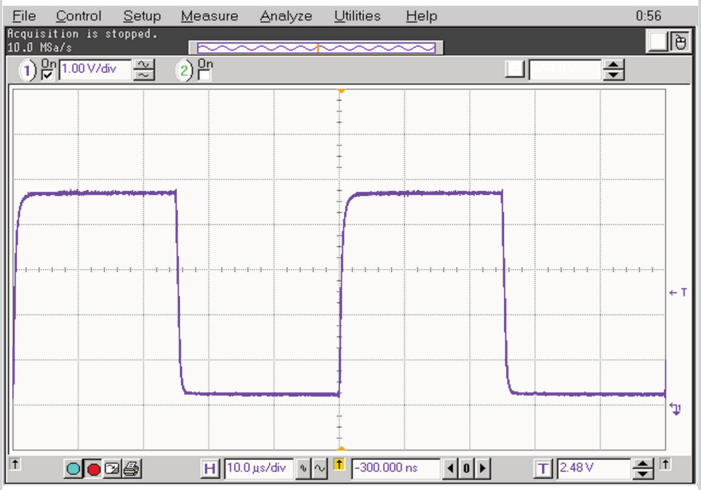

Figure 17.10.5: Measured output waveform.

	[4]	[5]	This work
Technology	0.1 µm CMOS (1P5M)	0.1 µm CMOS (1P5M)	0.35 µm/0.5 µm CMOS (2P4M)
VDD	1.5V (Logic) 5V (Analog)	1.5V (Logic) 5V (Analog)	5 V
Gray Scale	10b	10b	10b
Output Range	0V to 5V	0.25V to 4.75V	0.2V to 4.7V
DNL/INL	0.37LSB/1.71LSB	0.4LSB/0.7LSB	0.14LSB/0.61 LSB
Max. DVO	6.35 mV	20 mV	16 mV
Static Current Consumption	1.2 µA/channel	1 µA/Buffer	0.25 µA/DAC 0.93 µA/Buffer
DAC and Buffer Areas	206x14 µm²/DAC 127x14 µm²/Buffer	195x14 µm²/DAC 125x14 µm²/Buffer	530x28 µm²/DAC 150x28 µm²/Buffer
DAC Area Shrinkage (compared to 8b RDAC)	24 %	29 %	30 %

Figure 17.10.6: Performance summary.

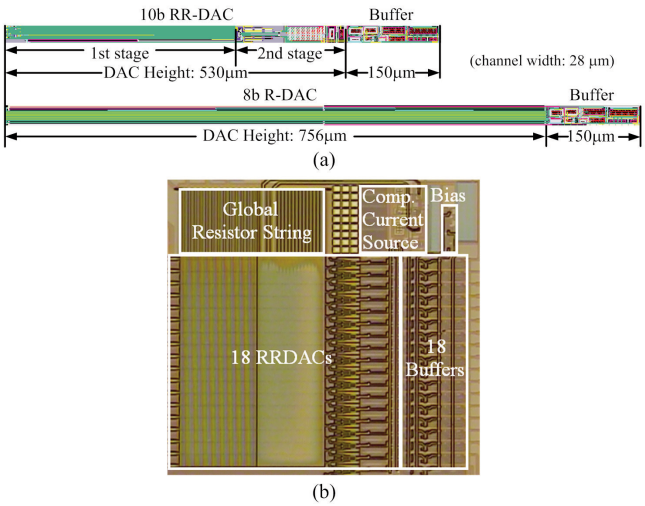

Figure 17.10.7: (a) Comparison of the layout dimensions between the 10b RRDAC and the conventional 8b RDAC. (b) Die micrograph for 18 RRDACs and 18 buffers.

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