16.10 183GHz 13.5mW/Pixel CMOS Regenerative Receiver for mm-Wave Imaging Applications

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Terahertz- and mm-Wave-based imagers have recently gained interest for imaging in security screening and bio-imaging applications [1,2]. For these applications to become practical, the core pixel circuits employed in an imaging array must meet challenging constraints that originate from the system level design and the needs of constructing large array structures on-chip. The most critical of these constraints is that the pixel must consume very low power, as an array will inflate the total power by n^2, where n^2 is the total number of pixels in a square (n x n) array. Pixel circuit area is the 2nd major constraint, as the single pixel area will be also inflated by n^2. This area constraint is critical because the cost-effective pixel array should ideally fit on a wafer to facilitate monolithic fabrication and avoid the need for complicated mechanical assembly of multiple array sections. A third system-level constraint similar to that experienced in CMOS image sensor arrays is the challenge of routing large numbers of analog signals between each pixel in the array and the sampling ADC.

For high-resolution systems (above 100x100 pixels) that operate in the mm-Wave spectrum, simultaneously meeting these three constraints becomes challenging, especially with traditional multiple-stage or heterodyne-based imaging receivers. This is because such receivers contain a large number of bias currents leading to increased power dissipation, and are constructed with a large number of passive devices, which consume a prohibitively large silicon area in the context of imaging array structures. A historically important alternative to the popular heterodyne and direct-conversion receiver architectures is the earlier developed super-regenerative receiver. Super-regenerative receivers are often used as non-coherent data receivers [3] in applications where power, cost, and area are extremely limited. Heterodyne and direct conversion architectures remain dominant in communications as they offer the advantages of coherent detection and recovery of phase information, enabling the quadrature signaling used by almost all modern wireless links. However, for mm-Wave imaging applications, there is no need or value in retaining phase information since imaging is based on power sensing only, making the super-regenerative receiver architecture a serious competitor in imaging applications.

In order for mm-Wave imaging to benefit from the advantages offered by the original super-regenerative architecture, we propose a new time-encoded regenerative receiver (TRR) architecture that is specifically adapted to meet the requirements of imaging array pixels. The proposed TRR uses digital CMOS circuitry to control a regenerative receiver and generate a time-encoded output signal. A block diagram of the proposed imaging receiver architecture with key waveforms is shown in Fig. 16.10.1. The proposed TRR receiver, when employed as the pixel element for an imaging array, directly addresses the three major constraints identified above:

1. TRR contains only two bias currents, greatly reducing power dissipation.
2. TRR is constructed with only two inductors, minimizing the pixel area.
3. TRR's time-encoded output can be routed by digital multiplexing rather than analog, greatly simplifying the pixel array interconnection.

Operation of the proposed TRR receiver is depicted in Fig. 16.10.1 and occurs as follows: When the digital clock edge arrives, the latch is set, engaging the oscillator. Once the oscillation envelope exceeds a designed threshold, the envelope detector is excited and resets the latch, terminating the oscillation. The super-regenerative principle (that an oscillator's startup time is inversely proportional to the log of injected power) suggests that the time between the latch set and reset is also inversely proportional to the input power.

Figure 16.10.2 shows the detailed schematic diagram of the TRR receiver implemented in 65nm CMOS technology. Transistor Q1 is biased by input transformer X1 and provides input injection into the oscillator stage from the antenna. Transistors Q2, Q3 and L1 form the oscillator tank and negative resistance element. The oscillator on/off control is provided at current source Q4, while Q5, Q6 and R1 form the envelope detector used to reset the digital latch. The latch itself is implemented as a standard CMOS digital logic block. The receiver contains only two DC bias currents, one flowing through Q1 and the other through Q4. As R1 is large (200kΩ), the DC current consumption of the envelope detector is negligible.

Unlike conventional imaging square-law detectors or LNAs, the regenerative nature of the TRR allows it to provide high gain, even at frequencies approaching f_{max}. This enables superior suppression of the TRR's flicker and thermal noise, resulting in a lower NEP than traditional imaging detectors (listed in Fig. 16.10.6). The TRR also offers excellent spectrum selectivity of less than 1% of the RF bandwidth, improving imager sensitivity. For active imaging higher sensitivity relaxes source power requirements, increases maximum target range, and enables the possibility of "false color" imaging at multiple frequencies.

To demonstrate the operation of the TRR receiver, an oscilloscope in eye-diagram mode is used to capture the time-encoded output, as an applied 183GHz input tone is switched between two power levels (-30 dBm and -50 dBm). As a result, the corresponding time-encoded output signal varies in pulse width by 1.0ns, as shown in Fig. 16.10.3. The sensitivity (-72dBm) position is also indicated.

To determine the TRR's bandwidth, a -50dBm tone is applied to the input and frequency swept through the receiver's bandwidth while the output time-encoded difference is plotted at each frequency in Fig. 16.10.4. If we consider a 50% change in pulse width to be the 3dB bandwidth of the receiver, then a receive bandwidth of 1.4 GHz is demonstrated by the measurement data.

To demonstrate imaging operation of the TRR receiver, two easily identifiable items are concealed inside cardboard boxes and illuminated with a 183 GHz 0dBm source (VDI). We then scan the cardboard boxes by using the CMOS TRR mounted on a digitally controlled moving mechanical stage with a target distance of 10cm. The mechanical setup and captured images are shown in Fig 16.10.5. Clearly visible through the cardboard box are the metal and plastic components of a computer floppy disk and a metallic wrench.

The measured TRR receiver performance is summarized in Fig. 16.10.6 along with a comparison to other state-of-art mm-Wave imaging receivers. The TRR sensitivity is measured directly by reducing the source power until the time-encoded difference is zero, and then computing the effective path loss. The NF and NEP are determined directly from the sensitivity and bandwidth measurements. The total TRR power dissipation is measured as 13.5mW/pixel while occupying only $1.31x10^4$ um^2/pixel of silicon area (not including antenna). Figure 16.10.7 shows the TRR die photo implemented in 65nm CMOS with an on-chip patch antenna. In the future, such an antenna can be constructed vertically above the TRR with spin-on polyimide as the interlayer dielectric.

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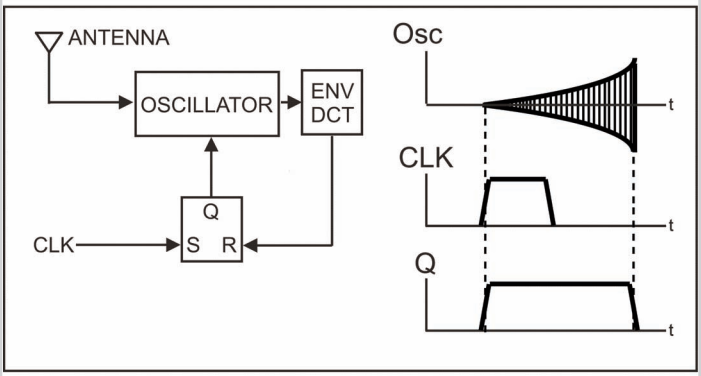

Figure 16.10.1: Time-encoded regenerative receiver (TRR) architecture and key waveforms.

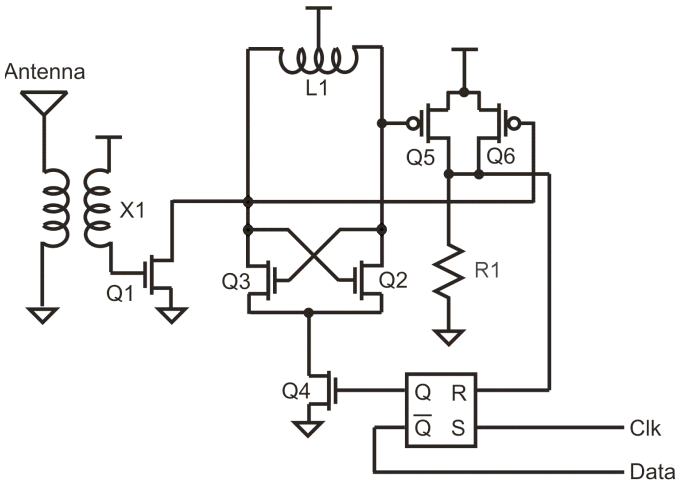

Figure 16.10.2: Time-encoded regenerative receiver (TRR) CMOS circuit implementation.

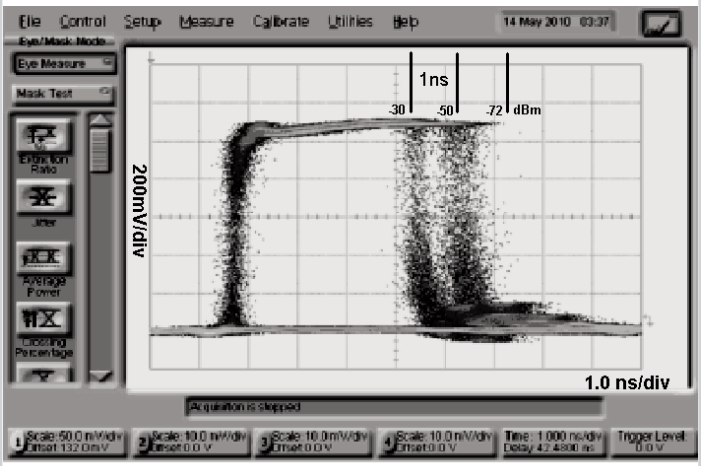

Figure 16.10.3: Eye-diagram waveform of TRR receiver for an applied 183GHz continuous-wave signal switching between –30 and –50dBm. Visible are two corresponding time-encoded pulse-widths (1.0ns difference).

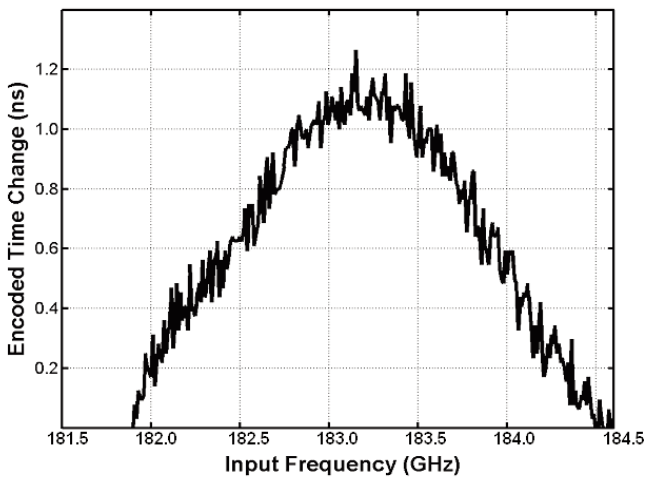

Figure 16.10.4: Frequency sweep of TRR showing receiver bandwidth. Power level of swept tone at -50dBm.

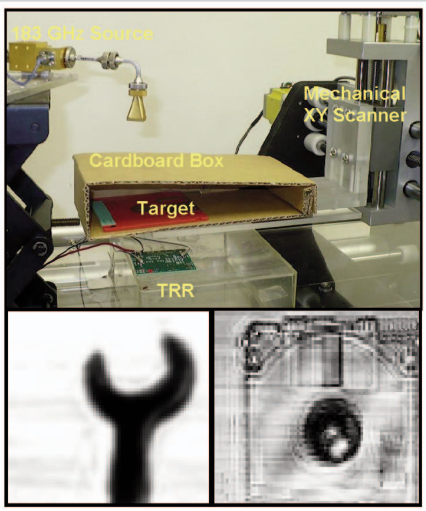

Figure 16.10.5: Mechanical setup and captured images of objects concealed in cardboard boxes when scanned by a TRR receiver pixel at 1mm/step resolution (left: adjustable wrench, right: 3.5" Floppy disk).

Receiver Characteristics	Value
Frequency	183 GHz
Power Dissipation	13.5mW / pixel
Peak Responsivity (time encoded)	1.3 ms/W
Pixel area	$1.31x10^4$ um^2 / pixel
Sensitivity	-72.5 dBm
Maximum Clock rate	150 MHz
3dB time-bandwidth	1.4 GHz
Noise Figure (NF)	9.9 dB (determined from sensitivity - KTB)
Noise Equivalent Power (NEP)	1.51 fW / $Hz^{0.5}$ (determined from KT[NF] $B^{0.5}$)

Receiver Characteristics	[1] MWCL 2008	[4] CSICS 2009	[5] RFIC 2010	[6] CICC 2007	This Work
Power Dissipation (mW/pixel)	250	39.6	200	93	13.5
Area (um^2/pixel)	Discrete	$4.1x10^5$	$1.25x10^6$	$3.02x10^5$	$1.31x10^4$
Output Format	Analog	Analog	Analog	Analog	Digital (Time-Encoded)
Frequency	580 GHz	94 GHz	94 GHz	94 GHz	183 GHz
NEP	N/A	200fW/$Hz^{0.5}$	10.3fW/$Hz^{0.5}$	N/A	1.51fW/$Hz^{0.5}$
Technology	GaAs	65nm CMOS	180nm SiGe	65nm CMOS	65nm CMOS

Figure 16.10.6: Performance summary and comparison with state-of-art imaging receivers.

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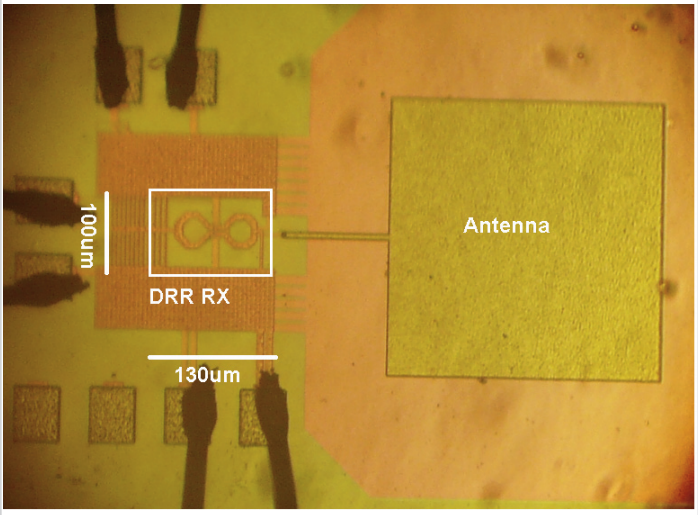

Figure 16.10.7: Die-photo of TRR receiver with half wave on-chip patch antenna.

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