200 GHz CMOS amplifier working close to device f_T

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A 200 GHz CMOS amplifier with a compact fully differential configuration is presented. Accurate device modelling and creative circuit design indicate the amplifier can support gain at frequencies close to device f_T. Measurement results are reported and validate the design by achieving 8.1 dB gain at 200 GHz and over 20 GHz positive gain bandwidth.

Introduction: The amplifier is one of the most critical building blocks inside communication systems, serving as the front-end to amplify small input signal and/or deliver large output power. Driven by ever increasing needs in portability, reliability and cost-effectiveness for high level system integration, the CMOS amplifier has started to attract attention in the millimetre-wave (mm-wave) and sub-mm-wave frequency range. Continuous deep-scaled CMOS also justifies such development by offering over 200 GHz f_T devices. A 150 GHz amplifier has been developed in 65 nm CMOS based upon a dummy prefilled micro-strip line, which achieves 8 dB gain and 27 GHz bandwidth [1]. Also [2, 3] reported development of over 100 GHz CMOS amplifiers. Nonetheless, they all construct single-ended architecture and hinder smooth integration into the single chip system owing to their poor immunity to supply/ground spurs and substrate couplings as well as excessive spurious generations. Therefore, this Letter reports a fully differential amplifier to reject common-mode noises/spurs that can work up to 200 GHz in 65 nm CMOS.

Circuit design: Although CMOS offers powerful integration capability and is ideal for implementing digital signal processing owing to scaling small size, low power consumption and high density, it is still handicapped for amplifier design in the sub-mm-wave regime because of the hefty parasitics, lossy substrate and inaccurate component models, especially when the working frequency is close to the device cutoff frequencies. Thus, tremendous efforts are needed for device optimisation and modelling. The mm-wave frequency device is highly layout dependent and the parasitics significantly affect circuit performance. Since existing models from foundries cannot represent devices accurately in such high frequencies, electromagnetic (EM) simulation tools, such as AnSoft HFSS, ADS Momentum, are utilised to characterise the connections through S-parameters. Together with the core device model provided by the foundry, a composite model can be created for a fair estimation of the real device performance inside the amplifier. Device sizing and optimisation is also based upon this model by evaluating the maximum available gain G_{MAX}, which indicates the device size of 10.32 μm/0.06 μm with 8 mA bias current could deliver the highest gain in 200 GHz.

Device f_{MAX} defines the maximum power gain frequency, which limits the frequency of voltage gain given perfect input and output matching. With good layout optimisation, device f_{MAX} is larger than f_T, which implies a positive gain could be achieved at the frequency close to device f_T. Fig. 1 depicts the proposed amplifier schematic intended to amplify the signal at such frequency. The amplifier features five cascade amplification stages. A coupled transformer is used to convey the signal, form inter-stage matching, isolate the DC voltage to allow independent optimisation for each stage and compact realisation [4]. The cascode amplifier structure is utilised to boost the reverse isolation and alleviate the amplifier stability concern without using the traditional RC compensation network.

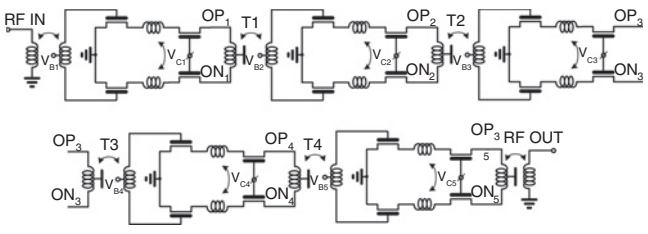

Fig. 1 *Schematic of proposed 200 GHz CMOS amplifier*

However, the cascode amplifier creates a short path to ground consisting of the stray capacitors from the amplification device's drain and cascode device source, together with the interconnect parasitic between them. In sub-mm wave frequencies, it becomes significant and appears as a lossy path, which degrades amplifier gain and power efficiency. To mitigate such lossy effect, a shunt inductor can be used to tune out the capacitor and boost the node impedance. However, this scheme has strong frequency selectivity by creating a high Q node within the amplifier, which conflicts with the broad band amplification requirement. Also, it is hard to align all five stages with the identical frequency owing to a lack of accurate active and passive component models, which otherwise could deteriorate amplifier performance.

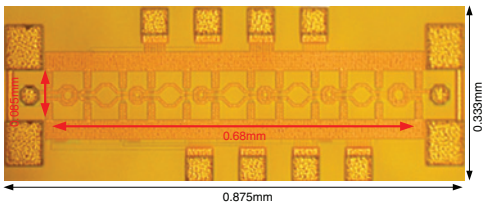

Fig. 2 *Chip micrograph*

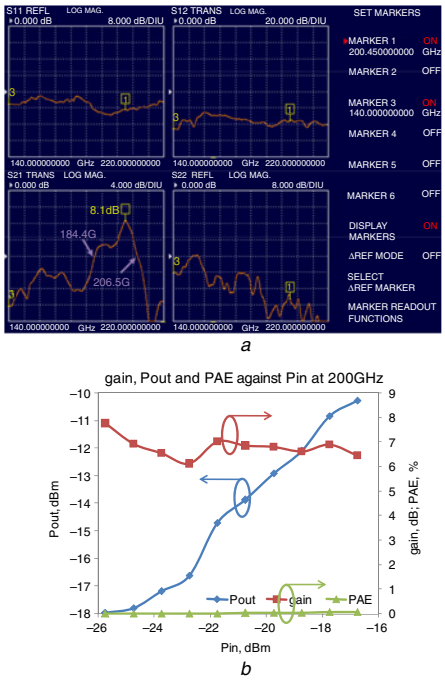

Fig. 3 *Measured S-parameters and Pout, gain and PAE against Pin*

a S-parameters
b Pout, gain and PAE against Pin

Series inductor/transmission line stub tuning proves to be more tolerant in frequency, which is inserted between stages and constructs a π matching network together with the device stray capacitors, as shown in Fig. 1. It transfers the impedance at the amplification device drain from the capacitive region into the inductive region, which provides conjugate matching with the cascode device source. This configuration mitigates the lossy capacitive short path and enhances amplifier gain and power efficiency by tuning out stray capacitors with slight linearity degradation owing to the higher impedance node between the amplification and cascode devices. Owing to its fully differential configuration, the amplifier's power supply rejection ratio (PSRR) has also improved by more than 12 dB in the desired frequency band compared with its single ended counterpart, validated by simulation.

Results: The amplifier has been fabricated in 65 nm RF CMOS, Fig. 2 shows the chip micrograph. It occupies 0.875 × 0.333 mm and 0.68 × 0.085 mm chip area with and without the PADs. To measure the amplifier performance in 200 GHz is not trivial owing to a lack of measurement instruments and setup delicacy. An Anritsu vector network analyser equipped with an OML G band module was used to measure the amplifier S-parameters as shown in Fig. 3. Compared with simulated

results, the peak gain frequency drops from 220 to 200 GHz and the gain is also lower from 14 to 8.1 dB. The amplifier achieves over 22 GHz positive gain frequency range. The measured input S11 is lower than −10 dB at 200 GHz and the reverse isolation is better than 35 dB.

The amplifier was also measured with a sub-mm-wave power source and a power sensor to characterise amplifier linearity and power added efficiency (PAE) at 200 GHz. Owing to limited source output power and excessive setup loss, the measured maximum amplifier output power is less than −10 dBm given −18 dBm input power after being de-embedded, which is lower than amplifier OP1dB and does not saturate the amplifier yet. The measured amplifier gain from this setup is around 7 dB, which is consistent with VNA measurement results. The calculated PAE is less than 0.09% mainly due to the small output power. The amplifier is biased with 2 V supply and consumes 108 mW power.

Conclusion: The reported design and experiment have demonstrated the feasibility of providing amplification at 200 GHz in 65nm CMOS, which is close to device f_T.

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One or more of the Figures in this Letter are available in colour online.

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