A Three Stage, Fully Differential 128–157 GHz CMOS Amplifier with Wide Band Matching

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Abstract—A fully differential amplifier has been realized in 65 nm CMOS technology, which has demonstrated 20 dB peak gain, over 10 dB gain from 128–157 GHz, and 40 GHz positive gain range from 126 to 166 GHz. By using cascode architecture with high bulk voltage tied to the cascode devices in deep-Nwell, the amplifier ensures stability and can use 2 V supply reliably. By inserting a π-matching network between cascode devices, it broadens the amplifier working range. This amplifier occupies 0.05 mm² chip area, delivers over 5 dBm output power, and consumes 51 mA from a 2 V supply. To the authors' best knowledge, this amplifier achieves the highest gain for CMOS amplifier beyond 100 GHz.

Index Terms—Cascode amplifier, CMOS, D-band, output $P_{1\,dB}$, PAE.

I. INTRODUCTION

MILLIMETER wave communication, radar, and imaging systems have drawn increasing attention due to the broad bandwidth that mm-wave offers and its unique capabilities to penetrate through fog/dust to detect concealed objects. Although CMOS has seldom been utilized in such a system before due to its inferior device speed, it has begun to gain ground with continuous scaled technologies. It has been proven that CMOS can achieve over 200 GHz frequency division [1], about 220 GHz fundamental frequency oscillation [2], and 140 GHz receiving for imaging applications [3]. On the other hand, the integration trend, mandated by ever increasing system needs for portability, reliability, and cost effectiveness, also calls for digital-compatible mainstream CMOS. The amplifier is one of the most critical and challenging blocks inside a transceiver. Therefore, we demonstrated a fully differential amplifier in 65 nm CMOS that offers gain from 126 to 166 GHz and achieves over 5 dBm output $P_{1\,dB}$.

II. CIRCUIT ANALYSIS AND AMPLIFIER DESIGN

A. Challenges in Mm-Wave Circuits

Although 65 nm CMOS could provide devices with $f_T >$ 200 GHz and $f_{MAX} > 250$ GHz [4], it still presents several

significant drawbacks to mm-wave circuits: lossy substrate limiting the passive component and transmission line quality factors, large gate/source contact resistance deteriorating transistor effective performance, and excessive parasitics eroding design margin and inducing inaccurate device modeling. In addition to these drawbacks, fully differential architecture is preferred for transceiver integration to alleviate noise and spurious coupling among digital, analog, and RF blocks. Several CMOS amplifiers operating over 100 GHz have been reported before [5]–[7]. A dummy-prefilled microstrip line [5] has been used to improve transmission line quality factor and circuit manufacturability. It uses simple matching topologies to deliver 8 dB gain and 27 GHz bandwidth at 150 GHz. Other literatures [6]–[8] also present amplifiers with a single-ended architecture that resists their deployment in integrated systems, where high gain and immunity to coupling noise are demanded.

B. Proposed Amplifier Structure

Fig. 1 depicts the proposed fully differential D-band CMOS amplifier. It features three-stage amplification and adopts a fully differential, cascode structure. Unlike single-ended amplifiers using capacitor coupling to separate dc voltage between stages, the proposed amplifier utilizes transformers to couple signal and enable independent bias optimization for each stage. To simplify testing, the amplifier has a single-ended input and output by using on-chip balun that transfers the single-ended signal into differential ones, and also presents 50 Ω matching network. The amplifier can be configured into fully differential arrangement by converting the baluns into transformers for transceiver integration [9].

Transformer coupling is an effective way to convey signal through stages and results in a compact implementation by merging inter-stage T-matching networks [10]. At higher frequencies, the transformer and balun become more efficient and can achieve >25 Q and >0.8 coupling coefficient. The transformer also offers design flexibility to adjust the signal swing by arranging its turn ratio to optimize performance, such as linearity. Although transformer is a powerful component in mm-wave regime, its usage is tricky due to its bi-directional coupling nature. This necessitates accurate transformer modeling and amplifier design iterations. Fig. 2(a) illustrates one monolithic transformer in a 65 nm CMOS 6-metal layer process, which is mainly formed by the 3.4 μm thick top metal and metal-4 and 5 as connection traces. Fig. 2(b) provides the associated model extracted by an EM simulation tool, ADS momentum.

Accurate device modeling is critical to mm-wave amplifier design. However, existing device BSIM3V4 model supported by foundry is dedicated to low frequency (<30 GHz) operation and cannot be directly applied. Therefore, an improved model
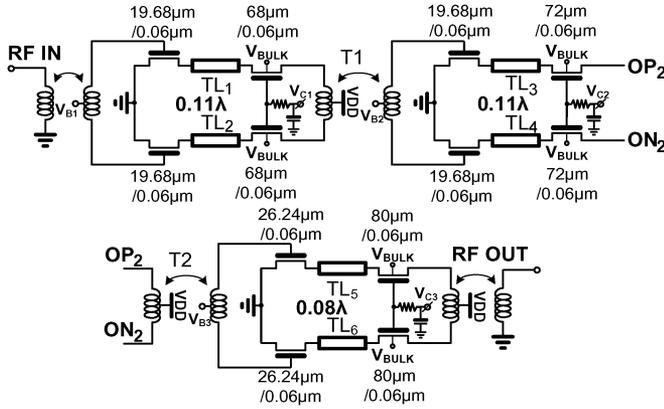
Fig. 1. Schematic of proposed D band amplifier.
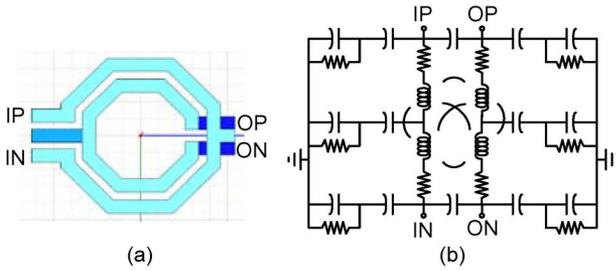
Fig. 2. (a) Monolithic transformer; (b) its physical model.
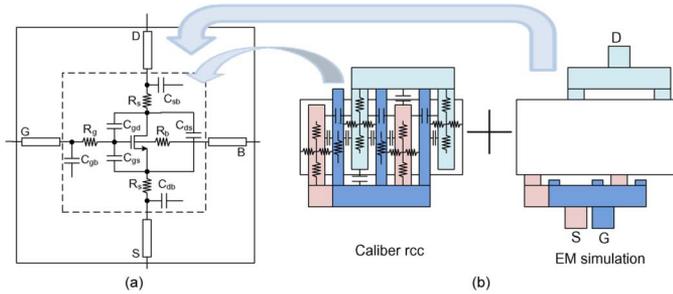
Fig. 3. (a) Mm-wave MOS device model; (b) core device model extracted by caliber RCX and metal wirings simulated by EM tools.

equipped with extrinsic parasitics is constructed, which includes the serial resistors of gate, source, and drain connection, coupling capacitors among them and the connection line effects. First, a core device is extracted by Caliber RCX to form a model core consisting of the transistor, poly connection resistors, and coupling capacitors; then the metal wirings are simulated with EM tools (i.e., ADS momentum) to incorporate the connection line effects. The ultimate mm-wave device model is formed by combining these two parts, as depicted in Fig. 3.

C. Amplifier Working Mechanism

Stability is a pronounced issue in mm-wave amplifiers, especially when designed for high gain. In a single transistor amplifier, the coupling between the input and output induced by Miller effect could form a positive feedback path. RC compensation network can be utilized to provide a stable amplification by mitigating the positive feedback at the cost of gain and power efficiency. On the other hand, cascode structure can also support unconditional stability by alleviating Miller effect. However, it
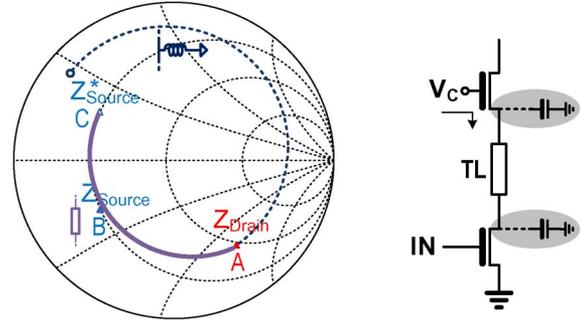
Fig. 4. Wideband inter-stage matching.

consumes precious voltage headroom and deteriorates linearity and amplification efficiency. To relax the voltage headroom, a high supply voltage, 2 V, is applied. Therefore, the cascode stage should adopt deep-Nwell device, and its bulk connects to a high voltage (∼1 V) instead of ground to ensure reliability. It also provides a large voltage swing to boost the amplifier linear output power.

Although cascode structure can improve amplifier stability by increasing the reverse isolation, it also creates a short path to ground through inner cascode node parasitic. It consists of the stray capacitors from the amplification device drain, cascode device source, and interconnect parasitics. At mm-wave frequency, it renders significant loss and degrades the amplifier gain and power efficiency. A shunt inductor can alleviate the loss by tuning out the capacitor and boosting the node impedance. However, this scheme induces strong frequency selectivity due to the relative high Q node, which conflicts with broad band amplification requirement.

Transmission line proves to be frequency-tolerant and can be inserted between stages and form a π-matching network together with the device stray capacitors, as shown in Fig. 4. It transfers the low impedance node A at amplification device drain from a capacitive region into node C in an inductive region, and provides conjugate matching with node B at the cascode device source. This configuration enhances the amplifier gain and power efficiency with slight linearity degradation due to the higher node impedance between the amplification and cascode devices.

III. MEASUREMENT RESULTS

The amplifier has been fabricated in 65 nm CMOS and occupies 0.1×0.48 mm^2 in core and 0.33×0.63 mm^2 with PADs, as shown in Fig. 5. To eliminate excessive parasitics, only top metal is used in the input and output PADs. To achieve high design accuracy, the PAD models are incorporated into the input and output matching networks. Because the input and output baluns isolate the on-chip active devices, the amplifier does not need extra protection and could also demonstrate great ESD performance.

Characterizing this amplifier is challenging due to the delicate measurement setup. A VNA with OML modules supports the D band S parameter measurement. A frequency multiplier chain generates a D-band signal, and a power sensor detects signal strength. They are used to measure the amplifier large signal characteristics together with a linearly adjustable attenuator with 50 dB dynamic range.
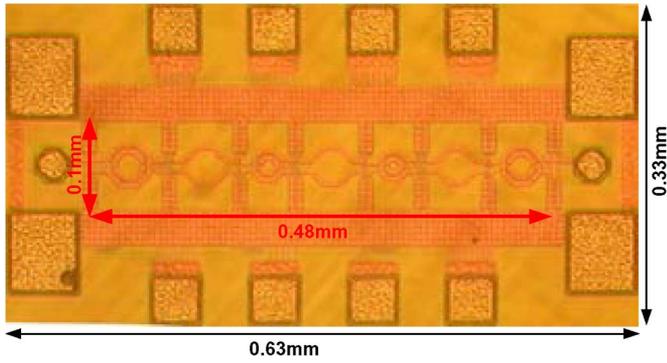
Fig. 5. Amplifier chip micrograph.
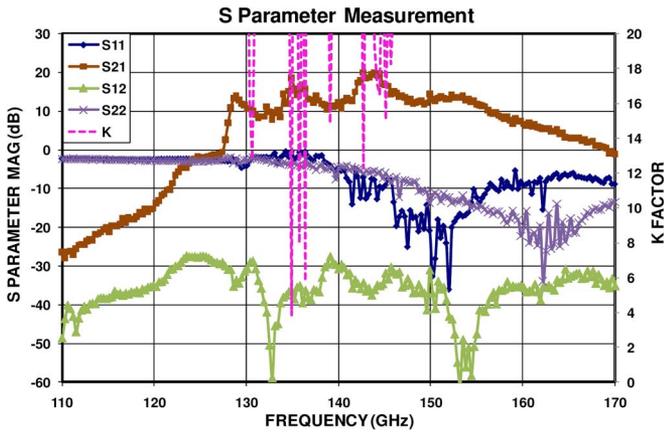
Fig. 6. Measured S parameters under 2 V supply.
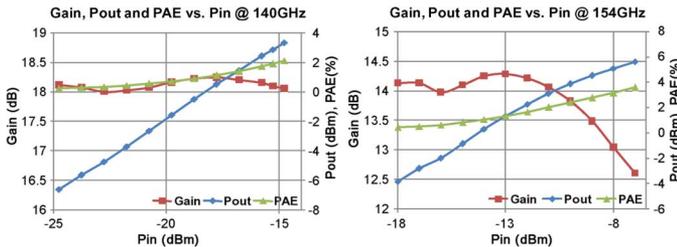
Fig. 7. Measured gain, pout and PAE.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[5]	[6]	[7]	[8]
Architecture	Differential	Single Ended	Single Ended	Single Ended	Single Ended
No. of Stages	3	3	6	3	5
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	90 nm CMOS	120 nm SiGe
Center Frequency (GHz)	144	150	140	103.8	135
3dB BW (GHz)	33GHz > 10dB Gain	27	10	5	20 GHz > 10dB Gain
Gain (dB)	20.6	8.2	8	9.34	20
Psat (dBm)	>5.7	6.3	>-1.8	N/A	N/A
P1dB (dBm)	5	1.5	-5	N/A	1
S11 (dB)	-24	-7.4	N/A	-9.8	N/A
S22 (dB)	-15	-13.6	N/A	-5.5	N/A
Power Consumption (mW)	54.6@1.4V 102@2V	25.5	63	22	112
Core Area (mm²)	0.05	0.16	0.06	0.24	0.08

can only deliver up to -14 dBm at 140 GHz and -7 dBm at 154 GHz. Thus we can only conclude that the measured amplifier saturated power is larger than 5.7 dBm and the peak PAE is higher than 3.6%, which are limited by the input signal power. The measured $OP_{1\,dB}$ is about 5 dBm. Table I summarizes the amplifier performance and compares it with the most recent D band CMOS/SiGe amplifiers. It verifies this amplifier achieves the highest gain with fully differential implementation.

IV. CONCLUSION

We have designed and validated a compact fully differential 128–157 GHz amplifier with over 10 dB gain and 20 dB peak gain in 65 nm CMOS. It also demonstrates 40 GHz amplification bandwidth with positive gain. The amplifier draws 51 mA from a 2 V supply and only occupies 0.05 mm^2 chip area. To the authors' best knowledge, it achieves the highest gain ever in the CMOS amplifiers operating over 100 GHz and paves the way for future integrated communication, radar, and imaging systems in D band frequency spectra.

Fig. 6 demonstrates the measured S parameters under a 2 V supply. It achieves better than -10 dB S11 from 142 to 157 GHz and larger than 10 dB gain from 128 to 157 GHz. Its positive gain range is from 126 to 166 GHz. The amplifier isolation is better than 25 dB and its S22 is less than -5 dB across the desired band. When the amplifier is biased with 1.4 V supply, its gain drops 2.5 dB. It is mainly introduced by the bias current decreasing from 51 mA under 2 V to 39 mA under 1.4 V, which reduces the devices transconductance. The amplifier shows high S11 and S22 at 130 GHz, while with 10 dB S21. It might be introduced by undesired coupling in layout, but no instability has been observed, as shown in Fig. 6. The measurement results matched simulations with ∼4 dB gain difference.

Fig. 7 shows the measured gain and output power versus input signal power after the setup loss is de-embedded. It confirms 18.3 dB gain at 140 GHz and 14.2 dB gain at 154 GHz. Due to the limitation of signal source and measurement setup, it

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