65 nm CMOS receiver with 4.2 dB NF and 66 dB gain for 60 GHz applications

N.Y. Wang, H. Wu, J.Y.C. Liu and M.-C.F. Chang

A direct conversion receiver for 60 GHz applications is fabricated in 65 nm CMOS. It consists of three low-noise amplifier gain stages, an RF mixer, a lowpass filter and a three-stage programmable gain amplifier. An overall minimum noise figure (NF) of 4.2 dB and maximum gain of 66 dB is achieved by the receiver occupying a core area of 0.26 mm^2 while drawing 36 mA of current from a 1 V supply.

Introduction: The 7 GHz of unlicensed band around 60 GHz has spurred intense research activities relating to low-cost, low-power and highly integrated circuits for applications in ultra-high data-rate wireless communications. Recent studies have shown deep-scaled CMOS to be a promising technology for achieving a cost-effective monolithic solution [1]. To enable high-order modulation schemes (i.e. 16QAM and above), the receiver noise figure (NF) must be sufficiently low. However, the low NF should not come at the expense of excessive power consumption for portable applications. Consequently, a compact, low-noise, low-power consumption receiver design is highly desirable.

Taking account of the above considerations, we have designed and implemented a low-noise, low-power receiver in 65 nm general purpose (GP) CMOS. As shown in Fig. 1, it is a direct-conversion receiver with a low-noise amplifier (LNA) tuned to 60 GHz followed by a mixer that down converts a RF signal to baseband with an external local oscillator (LO). The lowpass filter (LPF) and programmable gain amplifier (PGA) follow to complete the receiver chain. The prototype receiver achieves a maximum gain of 66 dB and a minimum NF of 4.2 dB with a compact area of 0.256 mm^2, while dissipating 36 mW DC power from a 1 V supply. On-chip high quality factor transformers and inductors with small form-factors are used extensively in the receiver to boost gain, interface between stages and provide DC isolation. To optimise the receiver gain and NF with the minimal power consumption, non-unity transformer turn ratio is utilised to enable either voltage or current amplification according to circuit needs.

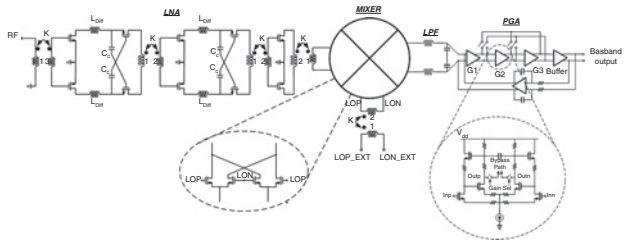

Fig. 1 *Schematic of 60 GHz direct-conversion receiver*

Circuit architecture: As shown in Fig. 1, the schematic of the receiver front-end consists of a fully differential transformer-folded cascode LNA and mixer to enhance the gain and linearity [2]. The receiver front-end has two stages of voltage amplification at 60 GHz followed by a transconductance stage that converts the amplified voltage into current and magnetically couples it via a transformer into the mixer's switching-quad. At its input, the LNA employs a 1:3 transformer for purposes of 1. matching, 2. voltage amplification, 3. single-to-differential conversion, and 4. DC isolation. The first two stages of the front-end adopt the differential cascode configuration for the best trade-off in gain, noise and stability. Differential inductors, L_{Diff}, are placed between the input and cascode devices to resonate out the parasitic capacitance. Cross-coupling capacitors, C_C, are applied to the differential cascode devices to boost g_m and reduce NF without current penalty [3]. A 1:2 transformer interfaces between the first and second stages with voltage magnification. Following that is a differential common-source transconductance stage that performs voltage-to-current conversion. A 2:1 transformer is placed between the transconductor and the double-balancing switching-quad with current amplification. A 1:2 transformer couples the LO to the switching-quad. The receiver front-end achieves 42 dB of conversion gain while drawing 14 mW from a 1 V supply.

Also shown in Fig. 1 is the schematic of the analogue baseband (LPF and PGA). The LPF is a passive second-order LC filter. The PGA has a maximum gain of 24 dB while drawing 22 mW from a 1 V supply. Its gain is distributed among three gain stages: G1 = 9.5 dB, G2 = 6.5 dB and G3 = 8 dB to optimise Rx linearity and NF. The last stage of the PGA is a buffer that drives an off-chip 50 Ω resistor. The buffer consumes 14 mW of power which accounts for 64% of the total PGA power (22 mW) for driving the 50 Ω load. However, in a fully-integrated radio, the PGA power consumption will be substantially lower because the ADC's input impedance is high. Finally, a DC-offset cancellation loop is used to prevent the PGA from saturating. Fig. 1 also details one of the PGA amplification stages. It consists of two stages of source-degeneration with active feedback to boost the output impedance. We can select the PGA gain by either connecting or bypassing stages.

Measurement results: The receiver was fabricated in 65 nm 1P6M process; Fig. 2 shows the die photo. The receiver front-end occupies an area of 0.123 mm^2 and the analogue baseband occupies 0.133 mm^2. Fig. 3 shows the measured conversion gain with all three gain settings against input frequency and the measured NF at the maximum PGA gain setting. The maximum gain achieved is 66 dB at 60 GHz. The minimum NF achieved is 4.2 dB at 60 GHz. The NF is measured using the Y-factor method. A V-band noise source (Quinstar, QNS-FB20PV) is inserted at the input of the receiver. The noise source is then switched on and off and the change in the output noise floor is read from the spectrum analyser. The change in the noise floor, expressed here as $Y = N_{ON}/N_{OFF}$, and the excessive noise ratio (ENR) provided by the manufacturer can be used to find the $NF = ENR/(Y - 1)$. Careful calibration of the cable losses is required for noise de-embedding.

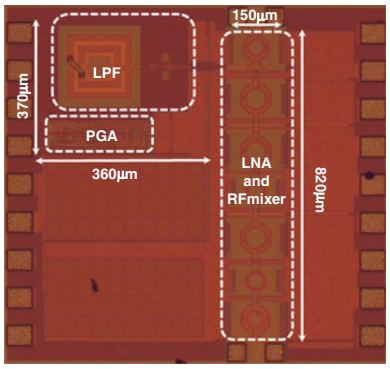

Fig. 2 *Die-photo of 60 GHz direct-conversion receiver*

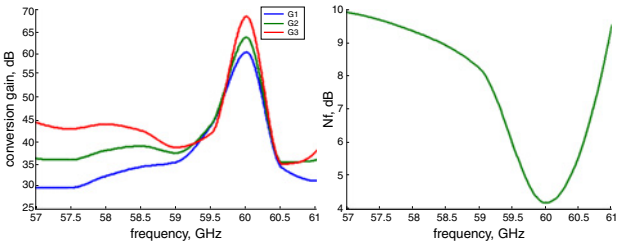

Fig. 3 *Measured conversion gain and noise figure of receiver*

Table 1: Comparison with prior arts

	This work	ISSCC'10 [1]	JSSC'09 [6]	ISSCC'08 [5]	JSSC'08 [4]
Conversion gain (dB)	***66***	35.5	14.7	55.5	30
Noise figure (dB)	***4.2***	5.6	5.6	6.1	7.1
Power dissipation (mW)	36/***22****	75	151	24	65
Supply voltage (V)	1	1	1.2	1	1.2
Area (mm^2)	***0.26***	2.4	1	1.55	1.4
Technology (nm)	65	65	65	90	90

*Without counting power dissipated by PGA's output buffer

The gain and noise figure variation across the spectra can be smoothened in future by staggering the band alignment at each resonating node. Nevertheless, both the gain and NF are sufficient in the band of interest. The simulated IIP3 and IIP2 for the receiver front-end are −49 and 9 dBm, respectively. The power consumptions of the front-end and the analogue baseband are 14 and 22 mW, respectively. Note that out

of the 22 mW dissipated in the analogue baseband, 14 mW originated from the output buffer that would be otherwise absent in a fully integrated radio with an on-chip ADC.

Conclusion: This work realises a 60 GHz CMOS receiver with a minimum noise figure of 4.2 dB, maximum gain of 66 dB while drawing 36 mA of current from a 1 V supply. Table 1 compares our receiver's performance with the state-of-the-art [4–6]. Our work exhibits the highest conversion gain, lowest NF, area, and DC power consumption.

3 November 2010
doi: 10.1049/el.2010.3094
One or more of the Figures in this Letter are available in colour online.

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