# CMOS Digital Controlled Oscillator with Embedded DiCAD Resonator for 58-64GHz Linear Frequency Tuning and Low Phase Noise

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***Abstract* — A digital controlled artificial dielectric (DiCAD) differential transmission line is embedded in 90nm CMOS to digitally tune a 58-64GHz DCO. DiCAD varies $\varepsilon_{r,eff}$ from 18.8 to 32.5. A shunt open stub DiCAD provides discrete capacitive tuning with 13.1° S11 phase variation. The core oscillator is an inductively loaded differential, cross-coupled NMOS pair. Large nonlinear varactors are avoided, and the phase noise is better than -90dBc/Hz at 1MHz offset. Linear tuning bandwidth of 9.3% with a 61GHz center frequency occupying 0.01mm$^2$ is achieved. Power consumption is 8.52mW with 1.2V.**

***Index Terms* — Slow Wave Structures, Permittivity, Digital Control, Voltage Controlled Oscillators.**

## I. Introduction

The current standards governing 57-65GHz wireless communication, such as IEEE802.15.3c, WirelessHD and ECMA, divide the band into four 2GHz channels [1]. Modulation rates and schemes vary, but each channel will be required to transmit and receive data at over 2GB/s between distances of less than 10m. Applications are for wireless HDMI cable replacement, uncompressed video and audio transmission and short-distance, high-speed bulk data transfer.

The success of these commercial standards is leveraged by the idea of a millimeter-wave chip set based upon the widely available low-cost, deep sub-micron digital CMOS process. Interest in this area has grown, and there are now many publications proving the viability of 60GHz CMOS front-end solutions, but none address the four channel requirement. The PLL and VCO in a direct conversion receiver/transmitter or directly modulated transmitter need to generate the four discrete center or carrier frequencies shown in Fig. 1.

CMOS VCO development efforts address the upcoming demand for low-cost and ultra-high speed wireless system applications in the 60GHz band. But, in order to cover the desired broadband, the VCO designs are typically based on a cross-coupled differential core with a standard L-C tank resonator and a large voltage biased varactor for frequency tuning. The nonlinear C-V characteristics of the large varactor is problematic because: 1) the PLL only uses the linear portion of the C-V curve which tends to limit the bandwidth coverage; 2) the tuning range can be further limited because of the varactor bias, which cannot exceed the CMOS power supply voltage (e.g. 1V in 90nm CMOS); and most importantly 3) the large $K_{vco}$ results in poor phase noise due to the direct modulation of the power supply noise.

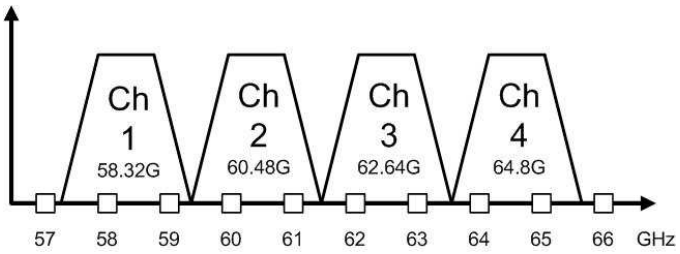


Fig. 1. IEEE802.15.3c Channel Plan

Band-selecting VCOs and mixed digital-analog PLLs have been introduced at low frequencies as a solution for low-phase noise wide-band signal generation. The VCOs combine digitally switched capacitor banks to move discretely throughout the band, and use a small varactor for continuous tuning. This limits the amount of up-converted noise through the varactor that degrades the VCO phase noise performance.

Previously, we demonstrated a 60GHz CMOS VCO using an embedded Artificial Dielectric (AD) resonator which can effectively reduce the oscillator's size, loss and phase noise (-100dBc/Hz at 1MHz offset). However, the CMOS tuning varactor limited the tuning range to less than 100MHz [2].

In this paper, we present a millimeter-wave digital controlled oscillator with a large tuning range and low phase noise that can be used as a basis for a band-select VCO and PLL. The discrete tuning is made possible by a digitally controlled artificial dielectric (DiCAD) rather than a MIM capacitor bank. Unlike the MIM capacitor bank, the DiCAD differential transmission line is a slow-wave structure easily modeled electromagnetically, well-characterized at millimeter-wave frequencies, and less susceptible to process variation since the standard MIM process uses an extremely thin high dielectric layer.

The DiCAD removes the frequency tuning constraint of our previous design and allows the DCO to accomplish a linear, discrete frequency tuning range of approximately 5.7GHz (or 9.3% of the 61GHz center frequency), while eliminating the disadvantages of nonlinear bias tuning and high phase noise associated with a large varactor.

## II. DiCAD

DiCAD was first introduced by authors in [3] to digitally control the effective permittivity, $\varepsilon_{r,eff}$, of a differential transmission line (DTL). The DiCAD transmission line

structure, as shown in Fig. 2 and implemented in the UMC 90nm 1P9M CMOS process, combines the top two metal layers M9 and M8 to implement a 2.25μm thick RF DTL, while using M7 and M6 to form the underlying periodic artificial dielectric floating strips. NMOS π-switches are then inserted along the virtual ground line of the DTL structure to bisect each of the floating strips. The switches are turned "on" or "off", "engaging" or "disengaging" the floating strips with the integral DiCAD to change its average effective dielectric constant $\varepsilon_{r,eff}$ from 18.8 (all switches off) to 32.5 (all switches on).

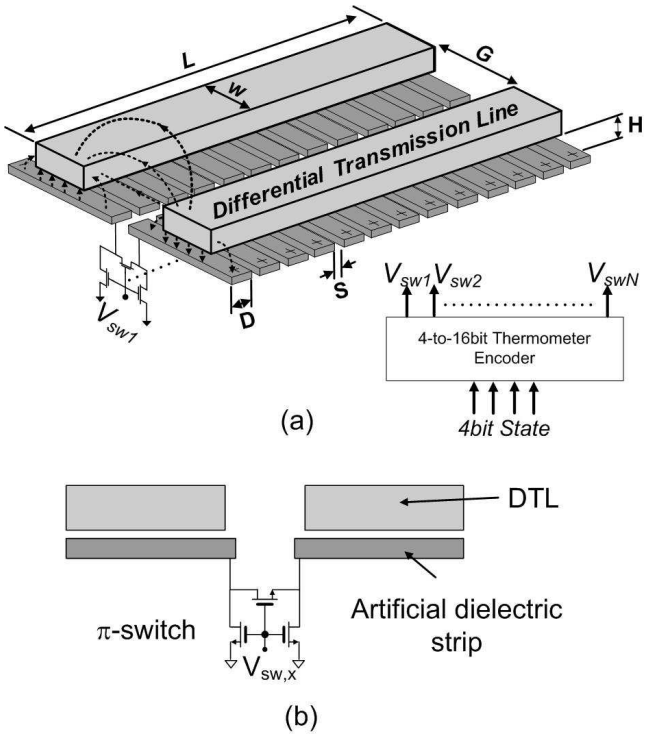


Fig. 2. (a) General DiCAD differential transmission line layout, (b) cross-sectional view of DiCAD DTL strip.

A 152μm DiCAD DTL test structure was characterized, and the effective dielectric constant was extracted at each state. A small digital thermometer encoder was integrated on the chip to toggle all 16 states. The DTL width, W, is 20μm, and the gap, G, 10μm. Increasing the size of W and G increases the effective dielectric constant as explained in [3]. The artificial dielectric strip width is 3μm and spacing is at a minimum 0.5μm. An Agilent 8371A network analyzer and custom SOLT calibration standards were used for testing. Most importantly, the effective dielectric constant exhibits a linear relationship with the digital state which is highly desirable. The phase varies linearly from -50.6° to -65.8°, though the phase is also dependent on impedance mismatch. In summary, the physics of the transmission line or more precisely its constitutive parameters are being digitally manipulated in a linear fashion using a standard digital CMOS process.

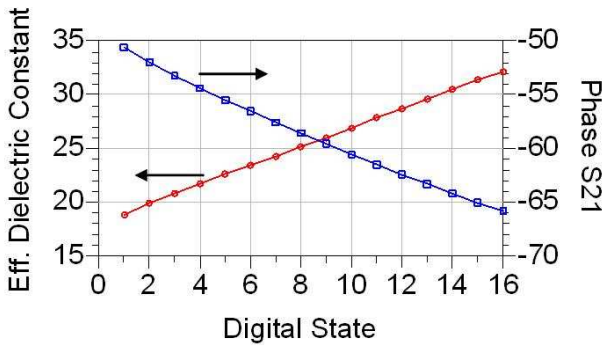


Fig. 3. Effective dielectric constant and S21 phase shift (deg) of a 152μm DiCAD DTL with 16 digital states. W=20μm, G=10μm, D=3μm and S=0.5μm.

## III. DCO Design

The DCO schematic is shown in Fig. 4. It is a standard cross-coupled NMOS pair loaded by a single-turn 58μm diameter inductor with a 5μm width and an open circuited DiCAD stub. The simulated Q of the inductor at 60GHz is 20.7, and the L value determined via the optimized $\Gamma_L$ from the stability circles. The cross-coupled oscillator core uses a CMOS pair with l=90nm, w=8μm and nf=4, while the open-drain buffers have w=4μm and nf=2 to minimize capacitive loading. Standard current mirrors bias the core and buffers.

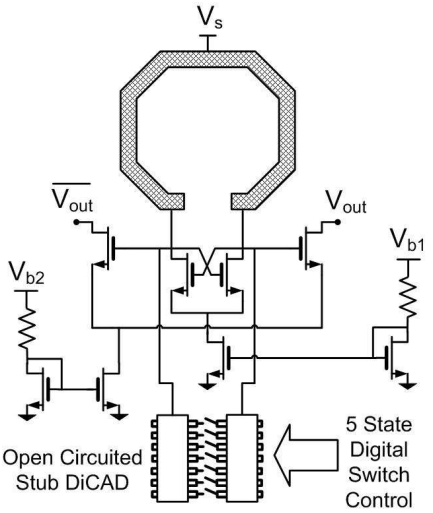


Fig. 4. DCO Schematic

Fundamental to the design is the use of the open circuited DiCAD stub as the tuning element. While linear, digital tuning is achieved there is a difference between short-circuited (S.C.) and open-circuited (O.C.) DiCAD stubs.

Thus far, DiCAD has been analyzed as a transmission line, but there is a unique property when it is utilized as a *reflective* element. It is clear that as the $\varepsilon_{r,eff}$ increases the phase constant, β, increases and the result is a larger magnitude

phase shift for a certain length. A second effect is the decrease in the characteristic impedance since it is inversely proportional to $\varepsilon_{r,eff}$ as well as the capacitance. What is not so apparent is that the impedance transformation or $S_{11}$ phase shift is *negligible (or insignificant tuning)* for an electrically short, short-circuited stub, since the characteristic impedance counters the increase in phase shift from β, while the opposite occurs for an open-circuited stub. It can be explained by approximating $Z_{in}$ with $Z_L$=0 for S.C. and $Z_L$=∞ for O.C. and tan(x) ≈x for small x. One concludes $Z_{in,O.C.}$ *varies* inversely to $\varepsilon_{r,eff}$ while $Z_{in,S.C.}$ is constant or exhibits *no change*.

$$Z_{in} = Z_0 \frac{Z_0 + jZ_L \tan(\beta\ell)}{Z_L + jZ_0 \tan(\beta\ell)} \quad (1)$$

$$Z_{in,O.C.} \approx -j\frac{Z_0}{\beta\ell} \propto \frac{1}{\varepsilon_{r,eff}} \quad (2)$$

$$Z_{in,S.C.} \approx jZ_0\beta\ell \propto \frac{\sqrt{\varepsilon_{r,eff}}}{\sqrt{\varepsilon_{r,eff}}} \propto 1 \quad (3)$$

Two 52μm long DiCAD test structures with 16 artificial dielectric strips were measured: (1) a short-circuited reflective stub, and (2) an open-circuited reflective stub. The DiCAD open-circuited stub shows over 26.2° $S_{11}$ phase shift, while the short-circuited stub exhibits 0° $S_{11}$ phase shift across all 16 states! Therefore, the open-circuited stub is used for the DCO.

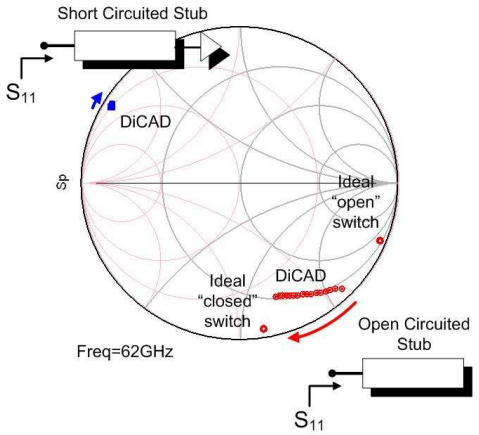


Fig. 5. S11 phase shift for O.C. and S.C. DiCAD elements.

## IV. Measured DCO Performance

Eight dielectric strips are used for the DiCAD open-circuited stub. Each two strip pair is connected to the same control line for a total of 4 input digital control lines and 5 discrete states: 0000 [zero "on" strips], 0001 [2 "on" strips], 0011 [4 "on" strips], 0111 [6 "on" strips] and 1111 [8 "on" strips]. The DiCAD DCO can tune to five different frequency points centered around 61.05GHz in our 1st design with a total tuning bandwidth of 5.56GHz tuning bandwidth, or 9.% of the center frequency, as shown in Fig. 6. The output power of the DCO is approximately -5dBm. The frequency range can be extended in our future designs to cover the whole bandwidth of 802.15.3c, and a small varactor maybe added for fine center frequency tuning.

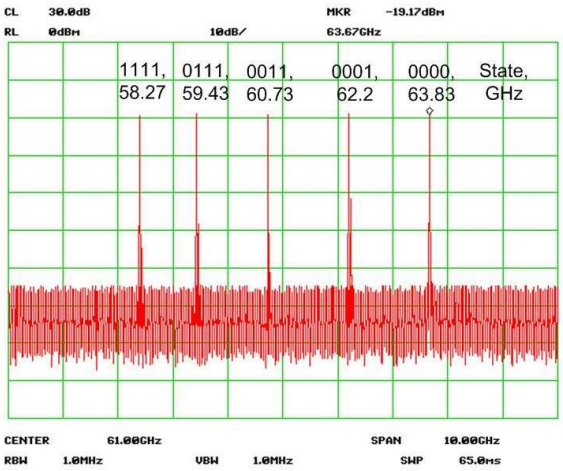


Fig. 6. DiCAD DCO generated frequencies.

A second VCO with a large varactor replacing the DiCAD element was also designed for comparison. The linear frequency tuning of the digital controlled open-circuited DiCAD is clearly evident versus the non-linear frequency tuning of the analog biased varactor as shown in Fig. 7. In practice, the varactor VCO is limited only to the linear range.

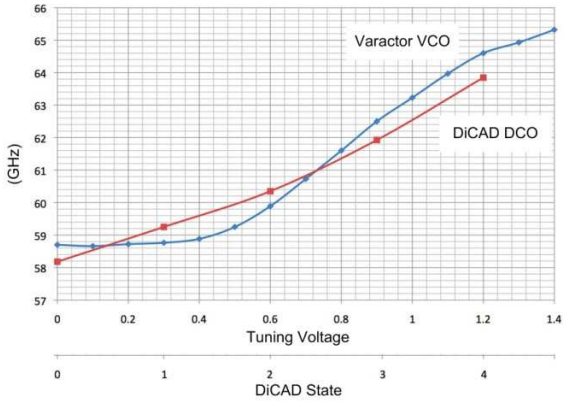


Fig. 7 Linear frequency tuning range of DCO compared with nonlinear varactor based design.

Most importantly, as shown in Fig. 8, the phase noise of the DCO is at -90dBc/Hz at 1MHz offset which is approximately 20dB lower than that of the varactor VCO.

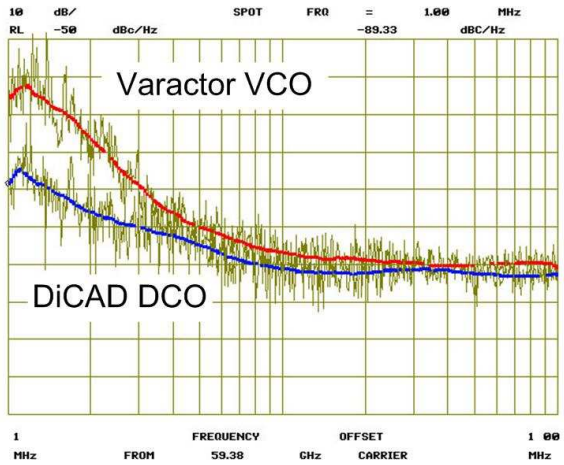


Fig. 8. Phase noise measurement between DCO and VCO.

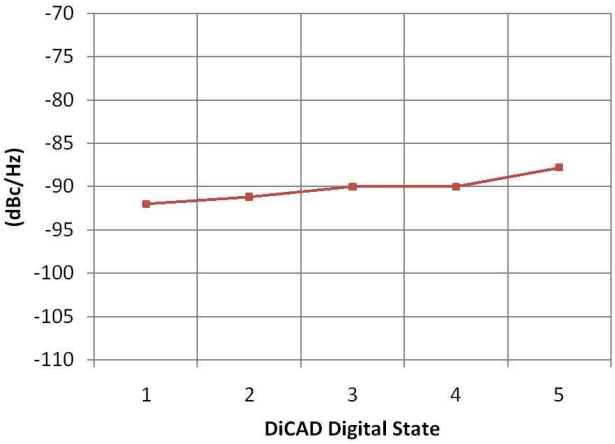


Fig. 9. Phase noise at 1MHz offset across the digital states.

The phase noise shows only a 4dB degradation when all the DiCAD switches are ON in Fig. 9. To gain some insight into why, we rewrite Leeson's equation as

$$L\{\Delta\omega\} = \frac{kTFR_P}{A^2}\left(\frac{\omega}{Q\Delta\omega}\right)^2 = \frac{kTF}{A^2 R_P}\left(\frac{\omega^2 L_p}{\Delta\omega}\right)^2 \quad (4)$$

where Q has been replaced by the equivalent tank resistance, $R_p$. If we assume that the Noise Figure, F, is constant and the oscillation amplitude is equal to a constant multiplied by the effective tank resistance, we may write:

$$L\{\Delta\omega\} \propto \frac{\omega^4}{R_P^3}. \quad (5)$$

Accordingly, the reduced frequency works to improve phase noise performance, while the additional loss from the ON switches will degrade it. Hence, there is only a slight degradation in phase noise with all switches on. Inductor series resistance and the gate resistance of the differential pair contribute to the loss and smoothes the variation in $R_p$.

The layout of the DCO is illustrated below in Fig. 10. It is extremely small with a core area of 0.01mm$^2$.

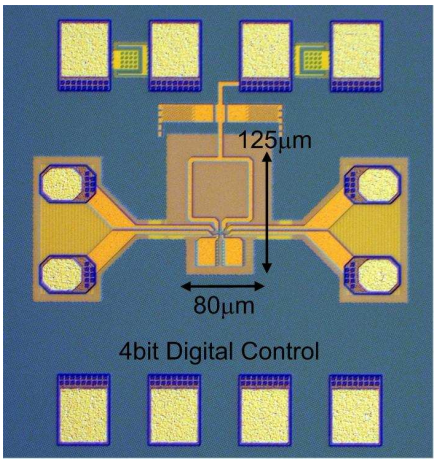


Fig. 10 DCO die photo.

## VII. Conclusion

The DiCAD DCO achieves a start-of-the-art $FOM_T$ when comparing with prior arts for the similar applications, and is a strong candidate for implementing digital and linearly reconfigurable millimeter-wave band-selecting VCOs.

| Ref. | Process | $f_0$ (GHz) | BW (%) | Phase Noise (dBc/Hz) | $P_{DC}$ (mW) | $FOM_T$ (dBc/Hz) | Core Area (mm$^2$) |
|---|---|---|---|---|---|---|---|
| DCO | 90nm CMOS | 61.05 | 9.27 | -90.1 | 10.6 | -174.90 | 0.01 |
| [4] | 65nm SOI | 70.2 | 9.55 | -83# | 10.15* | -169.46 | 0.027 |
| [5] | 0.13μm CMOS | 59 | 9.83 | -89 | 17.75* | -171.78 | na |
| [6]$^{\$}$ | 90nm CMOS | 49.95 | 7.01 | -87 | 10.4** | -167.71 | na |

*Added buffer current, **Reduced current by 0.5 since QVCO, #Estimated from plit, $^{\$}$QVCO
$FOM_T$=PN-20log($f_0$/Δf-FTR/10)+10log($P_{DISS}$/1mW)

Table I Comparison with prior arts.

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