60 GHz CMOS Amplifiers Using Transformer-Coupling and Artificial Dielectric Differential Transmission Lines for Compact Design

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***Abstract*—57–65 GHz differential and transformer-coupled power and variable-gain amplifiers using a commercial 90 nm digital CMOS process are presented. On-chip transformers combine bias, stability and input/interstage matching networks to enable compact designs. Balanced transmission lines with artificial dielectric strips provide substrate shielding and increase the effective dielectric constant up to 54 for further size reduction. Consequently, the designed three-stage power amplifier occupies only an area of only 0.15 mm^2. Under a 1.2 V supply, it consumes 70 mA and obtains small-signal gains exceeding 15 dB, saturated output power over 12 dBm and associated peak power-added efficiency (PAE) over 14% across the band. The variable-gain amplifier, based on the same principle, achieved a peak gain of 25 dB with 8 dB of gain variation.**

***Index Terms*—CMOS, differential amplifiers, millimeter-wave amplifiers, power amplifiers, transformers.**

I. Introduction

A CMOS transformer-coupled power amplifier and variable-gain amplifier for the unlicensed 57–64 GHz spectrum are presented with high efficiency and compact designs. The 60 GHz spectrum continues to grow in interest due to the anticipated demand for high-data rate, short-distance communication ($\leq$10 m) as well as the proven capability to fabricate a low-cost, high-f_t standard digital CMOS process [1]. It is widely recognized that CMOS is the technology choice in order to be successful in a high-volume market due its cost, however, the designs must be area constrained. Typically, millimeter-wave power and variable-gain amplifiers are designed using an expensive, high-performance, but less available III-V based semiconductor technology. The designs utilize standard $\lambda/4$ high-frequency passive structures such as a Wilkinson combiner or Lange couplers to effectively power combine single-ended designs, and the matching networks use long transmission lines. Unfortunately, cost and size are major drawbacks. This paper presents a methodology using on-chip artificial dielectric differential transmission lines and transformers to simultaneously achieve high performance and minimal size to allow a high level of integration within a low-cost 60 GHz CMOS transceiver.

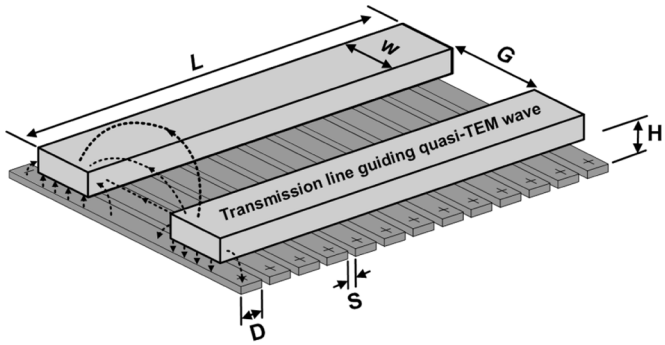

Fig. 1. Differential transmission line with floating artificial dielectric strips.

Artificial dielectric strips, as shown in Fig. 1, are inserted beneath a differential line [2], [3] and coplanar waveguide [4] on CMOS as a method to reduce the physical length of the transmission line by increasing the effective dielectric constant while simultaneously confining the electric field above the conductive substrate. Measurements confirm the improved loss per radian performance of a differential transmission line with artificial dielectric strips in Section II. Moreover, this technique is highly suitable for a standard, digital CMOS process with multiple metal interconnect layers (nine for the UMC 90 nm 1P9M). It is used in this paper as a differential line for the I/O feed network and output stub matching elements for the aforementioned purposes. The strips can dramatically increase the dielectric constant to above 54 even though the dielectric constant of silicon dioxide and of silicon is roughly 4.1 and 11.9, respectively. This new on-chip reactive technology is important as this paper advocates moving away from the traditional paradigm of single-ended designs using shielded microstrip or coplanar waveguide. This paper will also explain the critical differences between using artificial dielectric transmission lines for open and shorted stubs in impedance matching networks.

Transformer coupled power amplifiers have been introduced at lower frequencies [5]–[7], but only recently have transformers been used as a millimeter-wave element, [8]–[11]. In [9], we illustrated the effectiveness of the on-chip transformer in millimeter-wave CMOS power amplifier design for compactness and highest reported performance in efficiency, gain and associated saturated power. This is accomplished by combining the functionality of RF matching, stabilization and DC biasing

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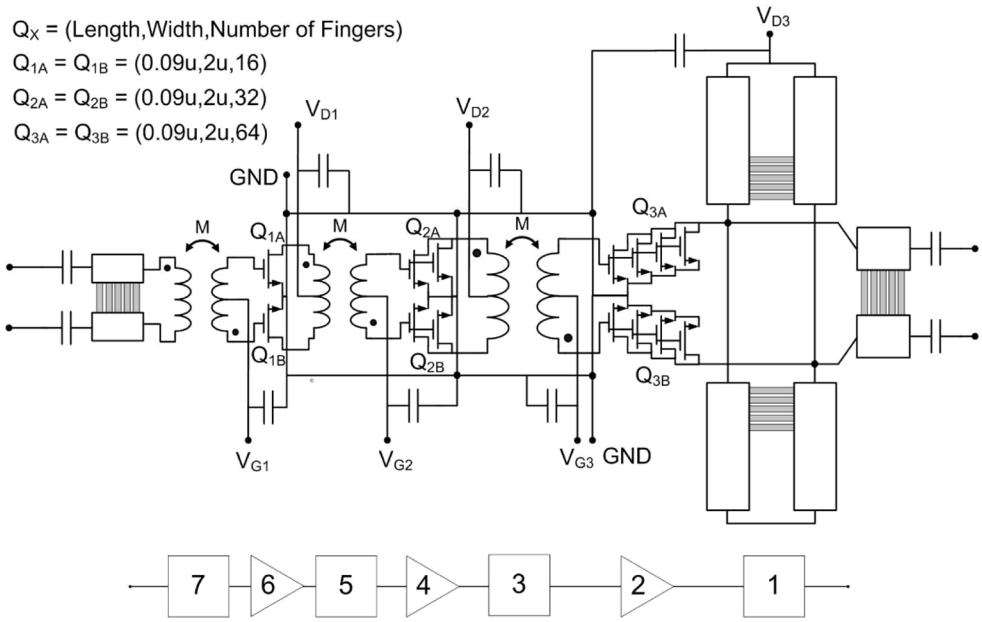

Fig. 2. Circuit schematic of differential, transformer coupled CMOS power amplifier.

networks in the transformer design. This paper examines the transformer performance with measured and simulated data, and gives a step-by-step discussion of its matching ability in amplifier designs. In addition, we report on a transformer coupled variable-gain amplifier in series with the power amplifier to further highlight the transformer as a millimeter-wave amplifier element. This circuit is the gain block for the system level transceiver design. In summary, unlike the traditional single-ended CMOS MMIC [12]–[16], the developed 60 GHz power and variable-gain amplifiers have exploited differential circuit architecture and taken full advantage of on-chip transformer coupling and artificial dielectric transmission lines to accomplish more effective impedance matching and power combining, higher output power and higher power-added efficiency (PAE) utilizing less silicon real estate consumption.

II. Architecture

The power amplifier is a three-stage, cascaded design using the UMC 90 nm 1P9M (nine metal layers) standard digital process with the schematic shown in Fig. 2. A common-source NMOS configuration with a 1.2 V supply voltage is used, maximizing current and voltage swings. The total gate peripheries of the pre-driver and driver stages are minimized in size to maintain a lower quiescent current and preserve efficiency with the exact value determined by analysis which will be elaborated on later. A differential transmission line and symmetric, shorted stub with on-chip artificial dielectric strips are used for the output match, while differential transformers are designed for inter-stage and input matching.

The variable-gain amplifier (VGA) is also a three-stage, cascaded design using the same process, but each stage is a differential cascode pair. A differential, cascode pair is a common topology for variable-gain design [17]. Gain variation is achieved by controlling the operating region (linear or saturation) in the common-source transistor Q_1 in Fig. 3. It is important to note that even though the cascode pair may offer some stability advantages, the layout must be well simulated to prevent the common-gate transistor from unwanted triggering of the amplifier instability. An inductor is inserted in series between the cascode pair to increase gain by improving the match between the capacitive loads, as well as to further improve stability. This concern for stability is important. In accordance with the Rollet Stability Factor and stability measure, the 90 nm gate length devices are only *conditionally* stable below 40–60 GHz, and thus are prone to oscillation if incorrectly loaded or by feedback, most likely through a bias line. We also emphasize the size reduction achieved by using on-chip differential transformers and artificial dielectric transmission lines for inter-stage and input matching functionality, as used in the VGA.

A. Differential Design Approach

The matching networks, input/output feed structures and lumped components are based on a two-port differential signal. This was chosen because it has ramifications on size, testing, biasing and even stability. We begin this discussion with the choice of passive transmission line technology. It is common to perceive CMOS microwave and millimeter-wave amplifiers with either a coplanar type waveguide or shielded microstrip, with the later being the most popular as shown in Fig. 4(a) and (b). The shielding is important to confine the electric field from penetrating the conductive substrate. It is usually used in a single-ended topology. This paper's amplifier is differential, so the shielded microstrip is not valid. The main reasons for using a differential approach is to take advantage of virtual grounds, as that adopted in a push-pull amplifier [18], and to interface with typically differential IF and baseband electronics. Gate and drain biasing can tap the virtual ground points of the transformer and the end of the shorted-stub as indicated in Figs. 2 and 3. This eliminates the need for a separate choke or

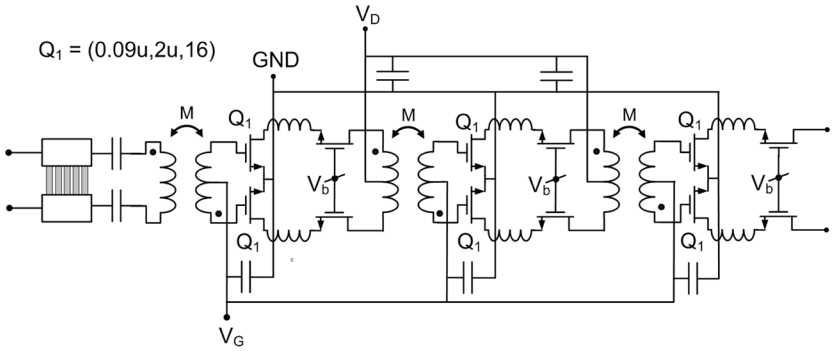

Fig. 3. Circuit schematic of differential, transformer coupled VGA.

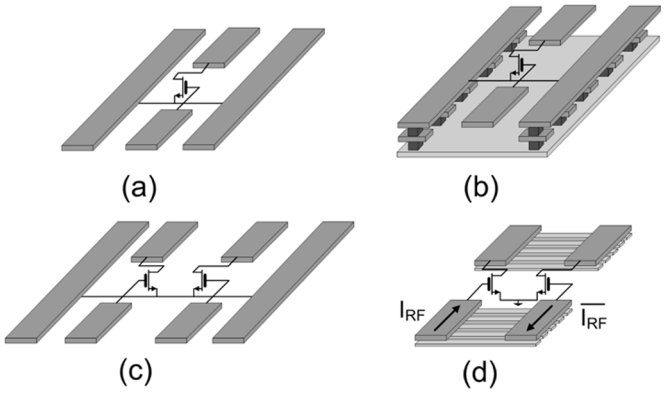

Fig. 4. Comparison of transmission line technology includes (a) coplanar waveguide, (b) shielded microstrip, (c) pseudo-differential, GSSG, and (d) artificial dielectric loaded differential coplanar strip, GS.

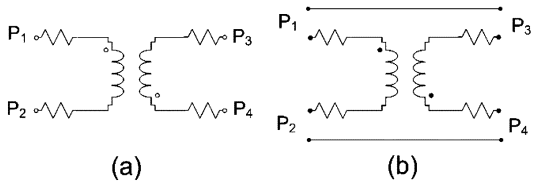

Fig. 5. Schematic of differential transformer (a) without ground shield and (b) with ground shield.

bias line. And, finally, it becomes clear that with little sacrifice of area the differential structure will add 3 dB more power versus the single-ended layouts; which is, in itself, a very strong reason to use the differential architecture. The not so obvious reasons follow: the standard differential approach usually is a four-port system with GSSG or GSGSG interfaces as shown in Fig. 4(c). This line can be driven with two independent sources 180° out of phase (pseudo-differential), or by adding an on-chip or off-chip balun. This works, but there are testing obstacles. If the design is a true four-port input (i.e., GSSG), then one needs either an expensive four-port network analyzer, or must take numerous measurements with a two-port network analyzer to extract mixed-mode S-parameter data which can be complicated. In large-signal testing, an off-chip balun is required, such as a magic-T, but it has -6 dB dividing loss so larger external amplifiers would be required, moreover all of the V-band interconnect cables cause phase and amplitude errors, so those must also be taken into account. All of this results in a difficult testing environment. On-chip baluns have similar drawbacks, such as phase error, and more importantly, their inherent loss would degrade gain, power, and PAE.

A simplified approach is taken in these designs by moving to a coplanar strip (GS) or differential mode with artificial dielectric strips transmission line in Fig. 4(d). The artificial dielectric strips provide electrical shielding and size reduction which will be explained in the next section. By removing reference ground lines, the signal *references itself* and reduces the area, resulting in a more compact design. The designs are driven by a two-port network analyzer or source with a *single GS probe (instead of GSSG)*, such as the I67-GS Infinity probe by Cascade Microtech. The RF currents launched from the input probe are equal and out-of-phase resulting in a true balanced or differential mode. This can be further explained by introducing the mixed-mode S-parameters derived in [19] and [20]. In a multi-port IO, the ports can be separately driven either in-phase (even mode) or out-of-phase (odd mode). In these designs, there is still a ground plane, so there are actually four ports and we can still use the equations for differential-mode S-parameters and odd-mode S-parameters, which are listed below.

$$S_{d1d1} = \frac{1}{2}(S_{11} - S_{21} - S_{12} + S_{22}) \quad (1)$$

$$S_{d1d2} = \frac{1}{2}(S_{13} - S_{23} - S_{14} + S_{24}) \quad (2)$$

$$S_{d2d1} = \frac{1}{2}(S_{31} - S_{41} - S_{32} + S_{42}) \quad (3)$$

$$S_{d2d2} = \frac{1}{2}(S_{33} - S_{43} - S_{34} + S_{44}) \quad (4)$$

$$S_{c1c1} = \frac{1}{2}(S_{11} + S_{21} + S_{12} + S_{22}) \quad (5)$$

$$S_{c1c2} = \frac{1}{2}(S_{13} + S_{23} + S_{14} + S_{24}) \quad (6)$$

$$S_{c2c1} = \frac{1}{2}(S_{31} + S_{41} + S_{32} + S_{42}) \quad (7)$$

$$S_{c2c2} = \frac{1}{2}(S_{33} + S_{43} + S_{34} + S_{44}) \quad (8)$$

Fortunately, we can electromagnetically simulate four ports (test is only two ports), and as an example, we can compare the two-port transformer (schematic in Fig. 5(a) and layout in Fig. 16) measurement data with the simulation. We use SONNET, a 2.5D full-wave electromagnetic simulator, to simulate the transformer as a four port model with each arm of

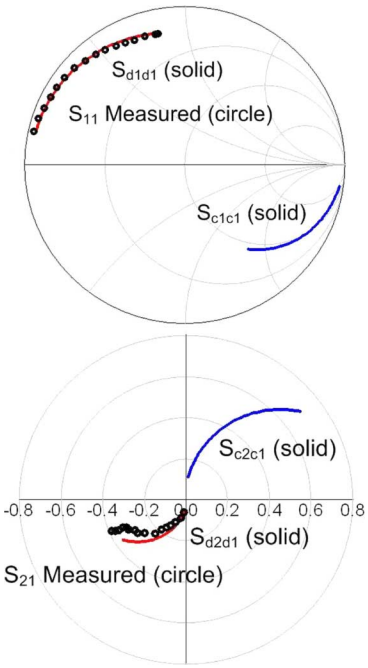

Fig. 6. Comparison of transformer measured (circle) data with simulated (solid) differential and common-mode S-parameters (a) S(1,1) and (b) S(2,1) from 10 GHz to 67 GHz.

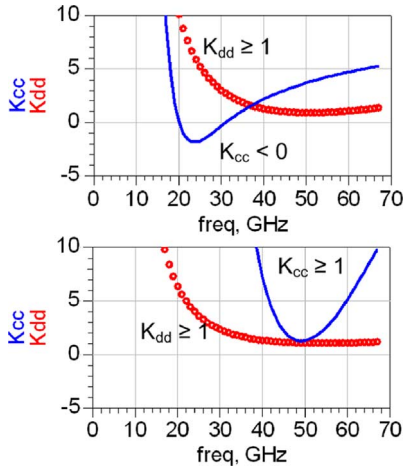

Fig. 7. Common-mode and differential-mode stability factors for (a) ground shielded transformer, and (b) non-ground shielded transformer.

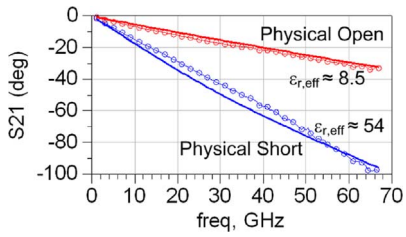

Fig. 8. S(2,1) phase shift for "physical open" and "physical short" differential transmission line. Simulation (solid line), and measurement (circles). W = 24 μm, G = 20 μm, D = 3 μm, and S = 0.5 μm.

the transformer assigned a port. The four-port simulated data is then transformed into the differential and common-mode S-parameters using (1)–(8). The result is shown in Fig. 6. The test data falls directly on the differential mode, which indicates that the GS test signal is a differential signal, and thus no baluns are needed. The GS test signal is not a simple RF signal and ground or (1,0) mode (again ± 1 V signal on one line, and 0 V ground on the uncoupled line). By reviewing even/odd mode analysis in [21] and [22], the (1,0) mode is actually a superposition of both the even mode (1/2,1/2) and odd mode (1/2,$-$1/2). If this were the case for the test signal, then the measured results would not have followed along the differential or odd mode at high frequency. The measured results prove a differential signal.

The final point addressed is amplifier stability between common and differential mode with regard to the GSSG and GS differential approach. The transformer in the previous example (see Fig. 16) was also simulated with a ground shield [Fig. 5(b)] to replicate a GSSG approach. Two separate single stage amplifiers: one with the ground-shield transformer and one without, differ by their stability. While the Q and inductance between the two are very similar, and the differential gains are both approximately 6 dB, there is a stability difference. By defining stability (K-factor [23]) for both modes using the following equations:

$$K_{dd} = \frac{1 - |S_{d1d1}|^2 - |S_{d2d2}|^2 + |\Delta_{dd}|^2}{2|S_{d2d1}S_{d1d2}|} \tag{9}$$

$$K_{cc} = \frac{1 - |S_{c1c1}|^2 - |S_{c2c2}|^2 + |\Delta_{cc}|^2}{2|S_{c2c1}S_{c1c2}|} \tag{10}$$

$$\Delta_{xx} = S_{x1x1}S_{x2x2} - S_{1x2x}S_{2x1x}, \tag{11}$$

the single-stage amplifier with the ground-shielded (GSSG) transformer exhibits a common-mode instability between 20–30 GHz, stability factor <0 in Fig. 7(a), while the GS transformer is unconditionally stable in Fig. 7(b). The extra ground line may cause an instability condition. In summary, the GS (coplanar strip), Fig. 4(d), differential approach is a more compact, straightforward, and generally a better performing approach.

B. Artificial Dielectric

Artificial dielectric originally was proposed in 1948 by W. E. Kock [24] as method to reduce the size of antenna lens, but only recently has this technique been introduced to CMOS [2], [3], [25]. In [2], two definitions are given for the case when the artificial dielectric strip is continuous as shown in Fig. 1, "physical short", and for the second case when the artificial dielectric strip is split midway, "physical open". In the UMC 90 nm CMOS process, if we compare the S(2,1) phase shift between a "physical short" differential line, and a "physical open" differential line, then we see about a 60° difference at 67 GHz as shown in Fig. 8. This corresponds to the effective dielectric constant increasing from 8.5 to over 54—more than six-fold increase.

The appropriate figure of merit for the transmission line loss should be (α/β) or (dB/rad) in order to take into account the reduced wavelength due to the increased permittivity. In Fig. 9, measurements confirm that the attenuation constant in dB/mm is the same for both the physical short and physical open structure with the same physical length. Both attenuation constants are

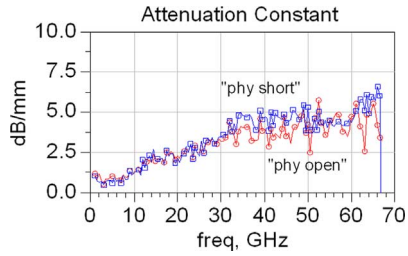

Fig. 9. Measured attenuation constants for "physical open" and "physical short" differential transmission lines.

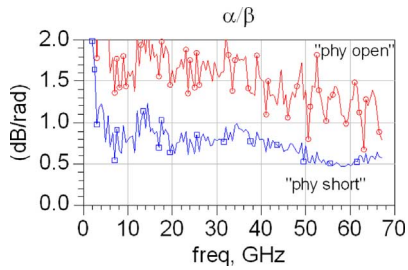

Fig. 10. Measured α/β or "physical open" and "physical short" differential transmission lines.

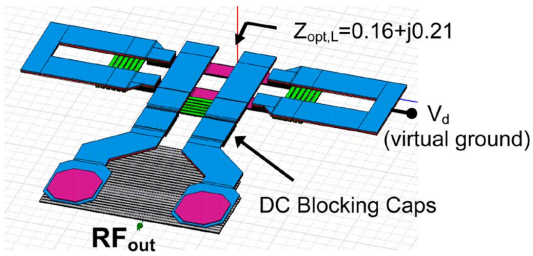

Fig. 11. Shorted-stub output matching network with artificial dielectric loaded differential transmission lines for power amplifier.

approximately 4 dB/mm. It seems that any loss prevention due to the electric conductive losses $\sigma|E|^2$ in the substrate is offset by resistive losses due to the strip itself.

Nevertheless, the major benefit of this slow-wave structure is more clearly evidenced as the attenuation constant is divided by the phase constant in Fig. 10. In the graph, the α/β decreases by 2.5× at 60 GHz. This shows that for the same phase rotation the loss is much less for the artificial dielectric loaded transmission line. Consequently, the power amplifier design benefits from these advantages by using the artificial dielectric differential line in the output match, as well as in the input/output transitions as illustrated in Fig. 11. The strips shield the substrate, reduce size, and can also control the impedance by using the strip dimension H as an extra design parameter besides G and W; Fig. 1.

It is important to recognize that artificial dielectric strips are *not* effective in a shorted-stub with a small line length. The test results for a 50 μm shorted-stub and an open-stub with both "physical open" and "physical short" artificial dielectric strips are shown in Fig. 12. The shorted-stub shows zero S11 phase shift between the two cases, while the open circuit is quite dramatic with over 58° phase shift at 60 GHz. Microwave transmission line theory shows that the effective dielectric constant

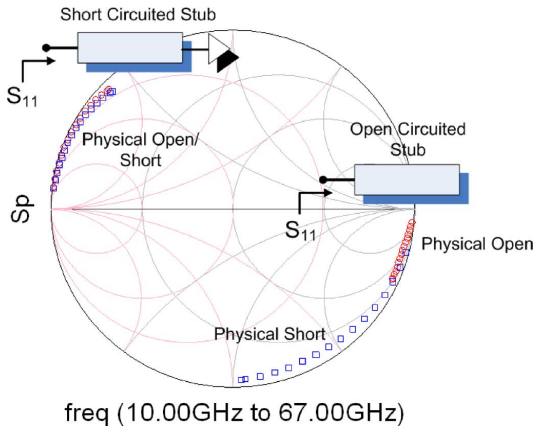

Fig. 12. Measured S11 phase shift for 50 μm shorted-stub and open-stub with both "physical open" and "physical short" artificial dielectric strips.

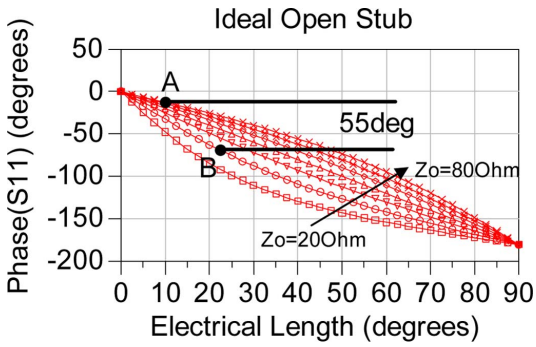

Fig. 13. S11 phase shift versus electrical length for various characteristic impedances (Z_O = 20 Ω: 80 Ω: 10 Ω step) of an ideal open stub.

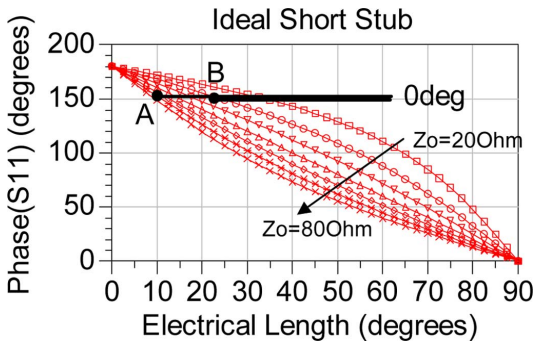

Fig. 14. S11 phase shift versus electrical length for various characteristic impedances (Z_O = 20 Ω: 80 Ω: 10 Ω step) of an ideal shorted stub.

of the artificial dielectric *increases* for both cases, but the characteristic impedances have an effect. Taking the equation for input impedance of a loaded line from [21] in (12), and substituting into (15) for a short and open loaded line to find S11, one can plot the relationship between the phase of S11 and the electrical length ($\beta\ell$) and the characteristic impedance as shown in Figs. 13 and 14. $Z_{0,X}$ is the characteristic impedance of the transmission line with either "physical short" or "physical open" artificial dielectric strips.

$$Z_{\text{in}} = Z_0 \frac{Z_L + jZ_{0,X}\tan(\beta\ell)}{Z_{0,X} + jZ_L\tan(\beta\ell)} \tag{12}$$

$$Z_{\text{in\_SHORT}} = jZ_{0,X}\tan(\beta\ell) \tag{13}$$

$$Z_{\text{in\_OPEN}} = -jZ_{0,X}\cot(\beta\ell) \tag{14}$$

$$S_{11} = \frac{Z_{\text{in}} - Z_0}{Z_{\text{in}} + Z_0} \tag{15}$$

The artificial dielectric changes both the effective dielectric constant and characteristic impedance of the line. Specifically, it *increases* the effective dielectric (or increases electrical length) and *decreases* impedance. Therefore, there are two cases for the 50 μm transmission line.

Case A: "Physical open" differential line: $Z_{0,\text{PhyOpen}} = 65\ \Omega,\ \beta\ell = 10°$.

Case B: "Physical short" differential line: $Z_{0,\text{PhyShort}} = 30\ \Omega,\ \beta\ell = 22.5°$.

These two cases are indicated on the plots as A and B. The simulated results are the same as the test. There is no phase shift for an ideal shorted stub, while there is 55° of phase shift for an open stub. It is therefore apparent, that in order to create phase shift for an open stub, the characteristic impedance must *decrease* and the electrical length increase which is ideal for an artificial dielectric differential line. Conversely, in a shorted stub the phase shift is created with an *increase* in the characteristic impedance and electrical length increase. Therefore, in the power amplifier output, the artificial dielectric is placed further from the shorted end of the stub for it to be effective.

C. Transformer Matching

A fundamental approach to microwave amplifier design is to first determine the correct input and output loading impedances whether it be for noise, gain, power, etc., and then design the matching networks. The majority of these networks are synthesized using well-defined distributed transmission lines suitable for microwave or millimeter-wave design [12]–[16]. Line parameters such as characteristic impedance, attenuation and electrical delay can be accurately analyzed with either closed form equations or numerically simulated with any electromagnetic software package. The line length, even at 60 GHz, is a limiting factor. A typical length of a quarter-wave line with a silicon substrate is on the order of 600 μm, which is significant considering the rule of thumb is 1 million digital gates occupy a 1 mm^2 area on a 90 nm digital CMOS process. The amplifier design presented here minimizes the size by folding the typical matching network including biasing as shown in Fig. 15 into a single, compact transformer as shown in Fig. 16.

In the power amplifier, the general goal of the matching network is to optimally load the input of the nth stage for maximum gain, and optimally load the nth-1 stage for maximum power transfer. These loads are determined via circle analysis using load and source pull techniques in a simulation or test environment. In Fig. 17, the third-stage load-pull power circles and second-stage maximum available gain circles are plotted on the smith chart. Overlaid on this chart are the impedances looking into the *loaded* transformer. It is apparent that the transformer successfully "transforms" the gate and drain impedances to $Z_{A,\text{Max}}$ and $Z_{L,\text{opt}}$. Fig. 18 illustrates the idea schematically. The transformer input, when loaded by the nth stage provides impedance that matches the optimum power load (via load-pull) of the nth-1 stage. Simultaneously, the transformer output when loaded by the nth-1 stage provides impedance that matches the optimum gain load of the nth stage.

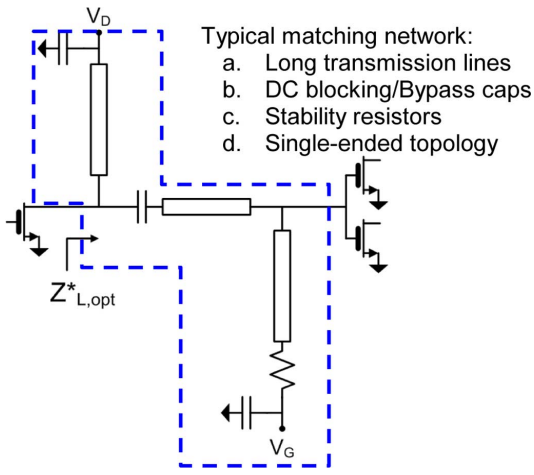

Fig. 15. Typical microwave transmission line matching network.

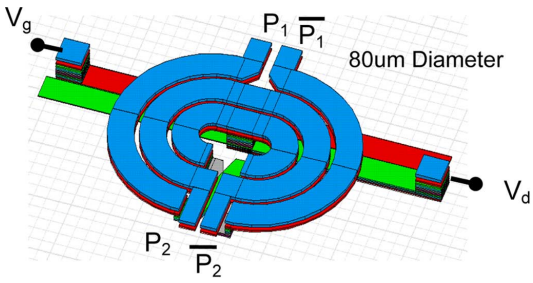

Fig. 16. Interleaved 2:1 transformer.

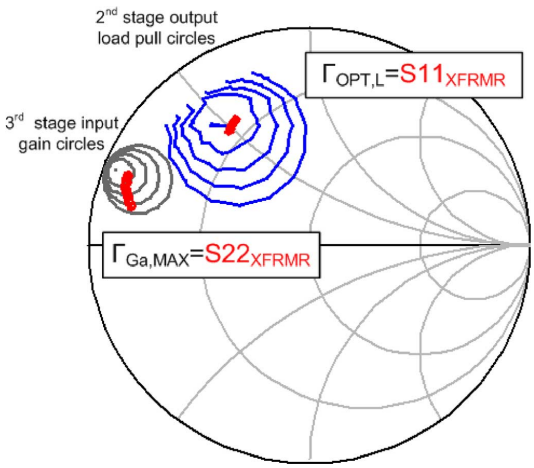

Fig. 17. Smith chart of load and gain circles of $n-1$ and n stage of power amplifier overlaid with transformer interstage match.

One can extract the component values using Z-parameters by viewing the transformer as a T-network. The effectiveness of the transformer can be visualized by plotting the path of the matching elements starting with the conjugate of $Z_{A,\text{MAX}}$. This is shown in Fig. 19. Starting with $S11_{Q3}$, a small series resistor and inductance moves the impedance to points b and c. The mutual inductance provides a larger shift since it is in parallel from c to d, followed by a large series inductor from d to e. This is important because in the power amplifier design, each stage

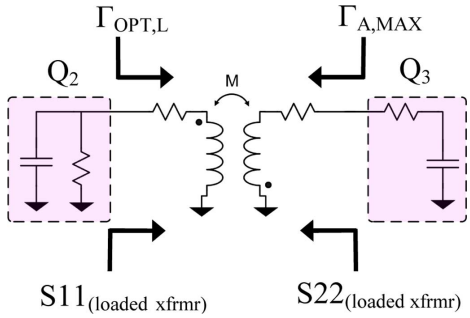

Fig. 18. Interstage transformer schematic with matching requirements.

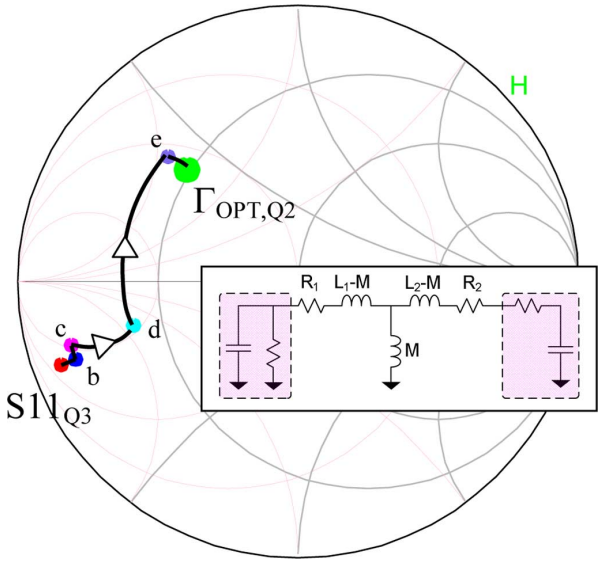

Fig. 19. Matching path of interstage transformer.

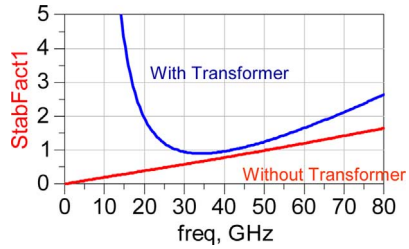

Fig. 20. Third-stage power amplifier stability with and without transformer.

is optimized for transistor size. This amplifier is designed for the last stage to move into large-signal saturation first, with each preceding stage moving into saturation approximately 3 dB later for maximum power delivery while maintaining high efficiency. Therefore, the transformer turn ratio is approximately equal to the transistor size ratio. This results in the series inductance $L_2 - M$, moving farther than $L_1 - M$.

The transformer also offers increased stabilization due to its resistance, coupling factor and inherent impedance. The stability factor, κ, must be greater than 1 across the entire spectrum starting just above dc (or 0 Hz) for each stage to maintain stability. This is usually accomplished by connecting in some fashion a shunt or series resistor. The transformer accomplishes the same task. As shown in Fig. 20, the stability factor for the third stage is dramatically increased to above one below 30 GHz, and improved elsewhere. This is understood with the T-model as well. The shunt inductance shorts the input voltage at low frequency and the inherent resistance stabilizes the device. The transformer combines matching, stability and bias networks and is therefore a feasible compact element for millimeter-wave amplifier design.

III. Design

This section reviews the design details by incorporating the topics from the previous sections into the design flow. The designs presented diverge from the traditional paradigm of single-ended amplifiers based on lengthy transmission lines toward differential designs utilizing transformers and artificial dielectric loaded lines with close attention to symmetry, parasitic resistances and compactness.

A right-to-left iterative design process is followed starting with device sizing in triangle 2, or T_2, in Fig. 2 where boxes, B_n, represent passive networks, and triangles, T_n, represent parallel active devices. Individual finger gate width was designed to 2 μm for suitable gate resistance that balances stability and gain, while the last stage total gate periphery of 256 μm was selected by load and source pull analysis. This is an iterative process testing performance across regions of the Smith Chart to determine the optimum load and source impedances of T_2 which are $Z_{2L,opt} = 0.16 + j0.21$ and $Z_{2S,opt} = 0.11 + j0.34$ at a class AB quiescent bias point. This bias point traditionally balances efficiency, gain and power, and was verified through simulation. Larger device sizes present challenges in achieving realistic matches below 10 Ω since positive gain is achieved via improving mismatch gain, since measured S21 without matching is less than 1 or negative gain.

It is important to note that most foundry models do not have gate and substrate resistances options activated for their standard digital nMOS and pMOS device bsim models, so the designer must determine these resistances, as well as parasitic capacitances, and externally add to the model or extract a new nonlinear model.

The last stage outmatching circuit, B_1, is a symmetrical, shorted stub with 20 μm wide lines and 10 μm gap to provide a high-Q network as well as handle 40 mA of bias current. The shorted-stub transforms the real output load to an inductive load of $j0.21$ which generally compensates the output capacitance. The characteristic impedance of the shorted stub is kept low since this helps decrease the inductance (further rotation on Smith Chart) and effectively shortens the line since $Z_{in} = jZ_o \tan(\beta\ell) \approx jZ_o\beta\ell$ for small $\beta\ell$ as shown in Fig. 21. Artificial dielectric strips lower the impedance to approximately 20 Ω resulting in a compact design.

The last stage transistor with its low impedance is the most sensitive to series resistance which will seriously degrade gain. Transformers, therefore, are not used due to the low self-resonance frequency and lower maximum available gain as compared to the shorted-stub as shown in Fig. 22. Custom 20 μm $\times$ 20 μm RF bypass parallel-plate capacitor using M3–M9 is placed prior to the stub to resonate the 100 μm GS probe launch inductance. The differential cross-section is designed to minimize the parallel capacitance. This makes up

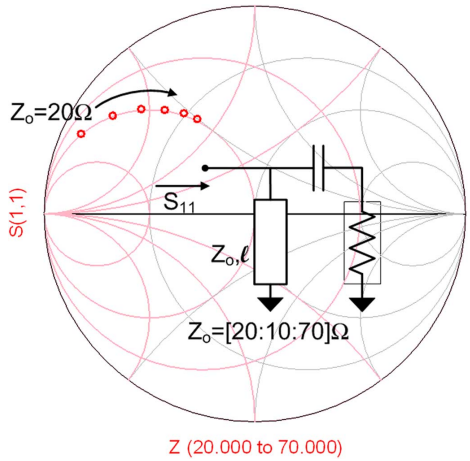

Fig. 21. Impedance transformation dependence on characteristic impedance of short-circuited shunt stub.

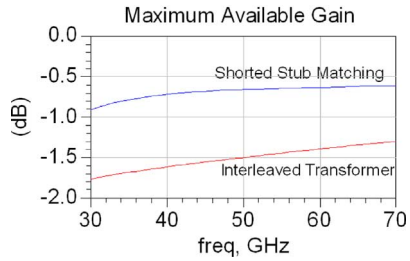

Fig. 22. Simulated maximum available gain of short-circuited shunt stub versus transformer.

B_1. A mandatory part of the design process is to electromagnetically simulate each part of the layout.

The physical dimensions of the artificial dielectric lines are initially estimated from the design curves discussed in detail in [2]. The strip spacing is kept to a minimum 0.5 μm, and strip-to-transmission line height minimized between M7 and M6, both for maximum effective dielectric boost. The strip width is an optimized value determined by the frequency. If it is too small, then the boost is limited, but it cannot be excessively large as it will become a larger fraction of the wavelength and boost will degrade. The design uses 3 μm. Finally, the larger gap dimensions increases boost due to the inductive increase and dominate fixed capacitance from the artificial dielectric strips. The gap is limited to 10 μm as a compromise between size and boost.

Next, the output transistor is simulated with a frequency dependent S-parameter output match, and more refined input impedance and overall gain are determined looking into $T_2\,B_1$. The driver, T_4, and pre-driver, T_6, transistor sizes are determined. These stages must not saturate prior to the output stage to avoid starving the power stage and becoming the dominate nonlinearity contributor. Usually

$$\mathrm{OIP3}_{n-1} = \mathrm{IIP3}_n + 6\,\mathrm{dB} \tag{16}$$

but this must be reduced to 3 dB since the gain is limited. Therefore, each stage is half the device size of the following stage.

Load and source pull is simulated for the driver stage, T_4, to determine the optimum impedances $Z_{4L,opt}$. The procedure

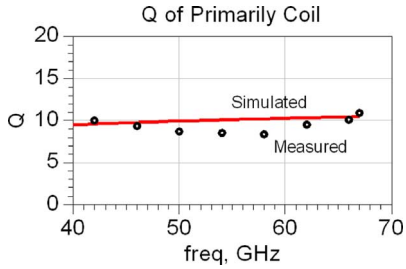

Fig. 23. Measured versus simulated Q of transformer's primary coil.

described in the transformer section is now followed to obtain B_3. It matches the input impedance of the output stage, T_2B_1, to the output match for the driver $Z_{4L,opt}$. The design flow is repeated for the pre-driver stage. Load and source pull for T_6 to determine $Z_{6L,opt}$. A more accurate driver stage input impedance is determined looking into $T_4B_3T_2B_1$, the transformer of B_5 is designed, and this is followed until the entire circuit, $B_7T_6B_5T_4B_3T_2\ B_1$, is completed.

Stability is usually addressed prior to matching, and the transistor generally is stabilized with a properly placed resistor. Unfortunately, most placements will somehow affect in-band performance and thus reduce gain. The gain per stage is roughly 5–6 dB so this absolutely cannot be lowered to maintain commercially viable performance. Therefore, the stability and input matching are simultaneously tackled by using the self-resistance of the transformer reflected in the Q to stabilize the transistor which is plotted in Fig. 23. So, stability is not addressed prior to matching, and it is not necessary to have such a high-Q transformer. The parallel mutual inductance to ground sets a very low impedance at lower frequencies, so any resistance in series with the transistor at either the gate or drain has a large dampening effect.

IV. RF Performance

The highest reported performance in PAE, power, and gain for a 60 GHz CMOS power amplifier is achieved in a very compact, low-power consumption design. The total first-stage current is approximately 10 mA, the second-stage current is 20 mA, and the third-stage is 40 mA. The supply voltage is 1.2 V with V_{GS} near 0.8 V. The current of the VGA varies between 5–25 mA with a 1.2 V supply.

A. Small-Signal

The typical power amplifier peak linear gain is greater than 15 dB centered at 61 GHz (Fig. 24) matching the simulation. The wideband response was tested with the Agilent 8731E network analyzer, and calibrated using the Picoprobe SOLT GS-67A calibration substrate. The simulated peak common-mode gain is -26 dB.

The VGA is actually in series with the power amplifier which is the gain block in the complete transceiver design. The peak gain is over 24 dB centered at 62.5 GHz with approximately 8 dB of gain variation. The variable-gain supply current varies from 7 to 22 mA. The results are provided in Fig. 25. The 3 dB bandwidth is reduced due to the number of stages, in future designs the stages will be limited to improve the VGA wideband performance.

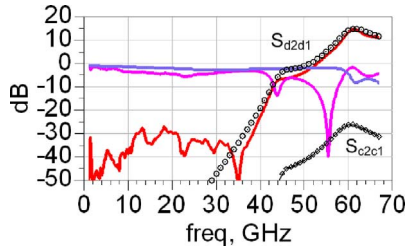

Fig. 24. Wideband linear response of CMOS power amplifier. Test (—), and simulation (∘). Simulated common-mode gain (♢).

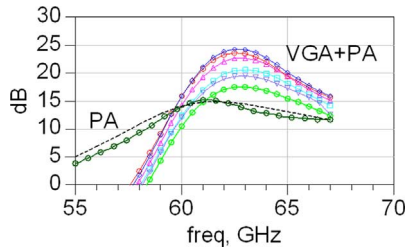

Fig. 25. Measured (circles) and simulated (dashed) small-signal gain of PA, and small-signal gain of VGA+PA with 7–21 mA supply current variation.

B. Large-Signal

Three different chips were tested. We used an Agilent 83640A synthesized sweeper that drives an 83557A 50–75 GHz mm-wave source module to generate the 57–65 GHz signal. This signal goes through a high-precision 50 dB variable waveguide attenuator, and amplified through a 60 GHz custom amplifier with GaAs MMICs from NGC. This provides up to 16 dBm linear output power, and is swept by changing the waveguide attenuator. A V8486 V-Band power sensor is used, and calibrated with the power meter after warming-up for an hour. The test amplifier is a golden standard, and validates the power sensing by checking the test amplifier's known output power.

We then accurately measure the swept input power before and after the probe tips that are connected by a short on-chip thru line using the Infinity I67 probes. The measured loss of the probe tips, coaxial to WR15 transition and on-chip launch is divided equally between the input and output, and is de-embedded from the raw measurements. The final step is to test the large-signal swept performance of the PA and VGA+PA. The error should be less than 0.5 dB.

The swept power performance for the power amplifier is shown in Fig. 26. $\mathrm{P_{1dB}}$ is 10.2 dBm, and $\mathrm{P_{sat}}$ is 12.2 dBm with an associated saturated power gain of 11 dB. PAE peaks above 19%.

Saturated power levels (Fig. 27) are consistent across the band generally above 10 dBm, and peaks above 12.5 dBm. $\mathrm{P_{sat}}$ extends beyond 65 GHz, and future designs can shift to a slightly lower center frequency.

The PAE (Fig. 28) is excellent across the band with a peak value over 20%, and exhibits a typical value of 14% for all chips. Last-stage drain efficiencies are close to 32%. The PAE variation is due to gain differences between devices most likely caused by process or corner variation.

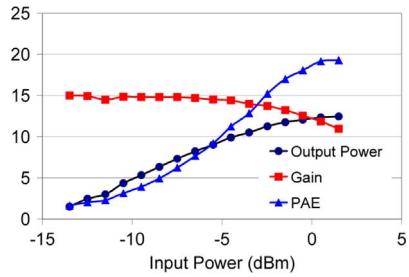

Fig. 26. Swept power performance including PAE (%), Output power (dBm) and gain (dB) of chip #1 at 63 GHz.

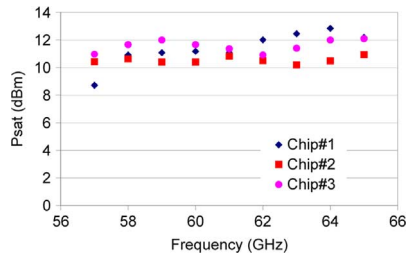

Fig. 27. Saturated output power of CMOS power amplifier.

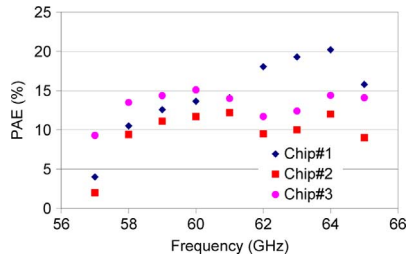

Fig. 28. PAE of CMOS power amplifier.

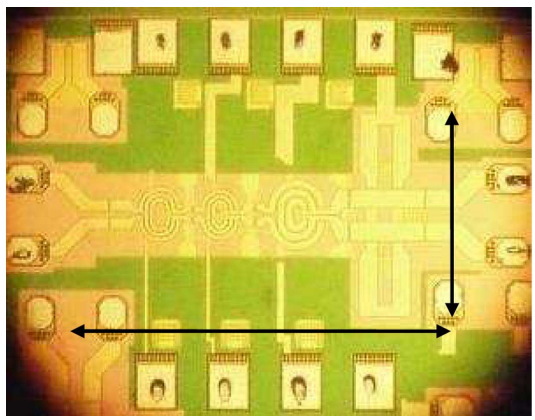

Fig. 29. 60 GHz CMOS power amplifier layout (0.5 mm × 0.3 mm).

V. Layout

The layout of the power amplifier is shown in Fig. 29. It is a compact design with an area of 0.15 $\mathrm{mm^2}$. The layout of the VGA in series with the power amplifier is shown in Fig. 30. Both utilize the low-cost, high-f_t standard UMC 90 nm 1P9M digital CMOS process, with nine metal interconnect layers.

When compared with a single-ended, transmission-line-based version that we designed a number of years ago, the new power amplifier design is 6× smaller in area, or 16.7% the area

TABLE I
COMPARISON OF PRIOR ART

Reference	**This Work**	*[13]*	*[11]*	*[16]*	*[15]*
Technology	**90nm CMOS**	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS
P_{SAT} (dBm)	**12.5**	8.4	12.3	10.6	8.4
PAE_{SAT} (%)	**19.3**	7	8.8	~1	5.8
$Gain_{SAT}$ (dB)	**11**	10.3	2.3	1	8.4
$Gain_{LIN}$ (dB)	**15**	15.2	5.5	8	17
V_D (volt)	**1.2**	0.7	1.0	1.2	na
P_{DC}(mW)	**84**	89	87	228.6	54
Area (mm^2)	**0.15**	0.18	0.26*	0.97*	0.99*

*Includes bondpads.

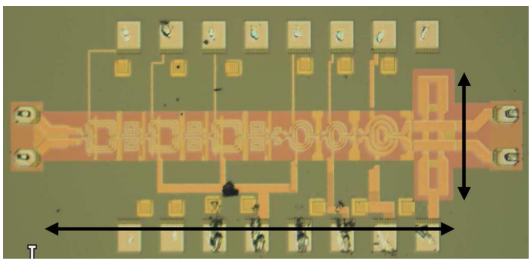

Fig. 30. 60 GHz VGA with power amplifier (0.925 mm × 0.3 mm).

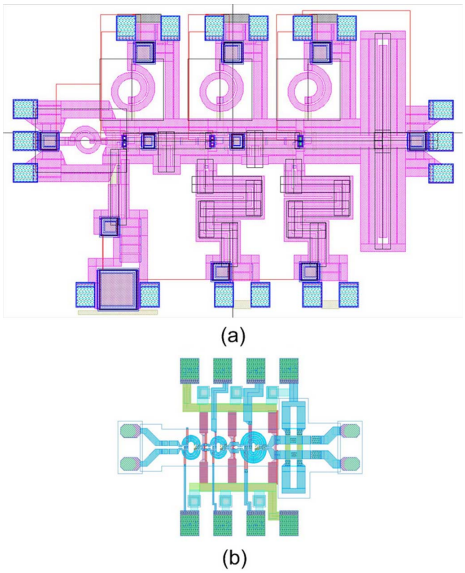

Fig. 31. Area comparison between (a) previous single-ended power amplifier design [0.75 mm × 1.2 mm], and (b) differential version [0.3 mm × 0.5 mm].

of the original version. Moreover, the new design significantly outperforms the older designs due to being smaller and differential. The gain is 7–8 dB higher and the saturated output power is 3.5 dBm greater. Fig. 31 compares the two layouts.

VI. CONCLUSION

Comparing this paper to prior papers in Table I, this paper presents the highest reported performance in terms of saturated power (12.5 dBm), PAE (19.5%), and linear/saturated gains (15 dB/11 dB) for a 60 GHz CMOS power amplifier. The power amplifier is implemented in differential circuit architecture, and utilizes on-chip transformers and artificial dielectric transmission lines to achieve a compact design. The design is shown to be stable and repeatable.

ACKNOWLEDGMENT

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REFERENCES

[1] *RF and A/MS Technologies for Wireless Technologies*, ITRS Roadmap [Online]. Available: http://www.itrs.net/

[2] T. LaRocca, S. Tam, D. Huang, Q. Gu, E. Socher, W. Hant, and F. Chang, "Millimeter-wave CMOS digital controlled artificial dielectric differential mode transmission lines for reconfigurable ICs," in *IEEE Int. Microwave Symp. Dig.*, 2008, pp. 181–184.

[3] W. Andress and D. Ham, "Standing wave oscillators utilizing wave-adaptive tapered transmission lines," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 638–651, Mar. 2005.

[4] T. S. Cheung, J. Long, K. Vaed, R. Volant, A. Chinthakind, C. Schnabel, J. Florkey, and K. Stein, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *IEEE ISSCC Dig. Tech. Papers*, 2003, pp. 396, 501.

[5] J. G. McRory, G. Rabjohn, and R. Johnston, "Transformer coupled stacked FET power amplifiers," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 157–161, Feb. 1999.

[6] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, "Distributed active transformer—A new power-combining and impedance-transfromation technique," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.

[7] W. Simburger, H. Wohlmuth, and P. Weger, "A monolithic transformer coupled 5-W silicon power amplifier with 59% PAE at 0.9 GHz," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1881–1892, Dec. 1999.

[8] T. LaRocca, "60 GHz CMOS differential power amplifier using on-chip transformers for in-phase power combining and compact design," in *UCLA Annual Research Review*, 2006.

[9] T. LaRocca and F. Chang, "60 GHz CMOS differential and transformer-coupled power amplifier for compact design," in *IEEE RFIC Symp. Dig.*, 2008, pp. 65–86.

[10] D. Huang, R. Wong, Q. Gu, N. Wang, T. Ku, C. Chien, and F. Chang, "A 60 GHz CMOS differential receiver front-end using on-chip transformer for 1.2 volt operation with enhanced gain and linearity," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2006, pp. 144–145.

[11] D. Chowdhury, P. Reynaert, and A. Niknejad, "A 60 GHz 1 V +12.3 dBm transformer-coupled wideband PA in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 560–561.

[12] B. Heydari, M. Bohsali, E. Adabi, and A. Niknejad, "Millimeter-wave devices and circuit blocks up to 104 GHz in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2893–2903, Dec. 2007.

[13] M. Tanomura, Y. Hamada, S. Kishimoto, M. Ito, N. Orihashi, K. Maruhashi, and H. Shimawaki, "TX and RX front-ends for the 60 GHz band in 90 nm standard bulk CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 558–559.
[14] Y. Jin, M. Sanduleanu, and J. Long, "A wideband millimeter-wave power amplifier with 20 dB linear power gain and +8 dBm maximum saturated output power," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1553–1562, Jul. 2008.
[15] D. Dawn, S. Sarkar, P. Sen, B. Perumana, D. Yeh, S. Pinel, and J. Laskar, "17-dB-gain CMOS power amplifier at 60 GHz," in *IEEE Int. Microwave Symp. Dig.*, 2008, pp. 859–862.
[16] T. Suzuki, Y. Kawano, M. Sato, T. Hirose, and K. Joshin, "60 and 77 GHz power amplifiers in standard 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 562–563.
[17] H. D. Lee, K. Lee, and S. Hong, "Wideband VGAs using a CMOS transconductor in triode region," in *Proc. European Microwave Conf.*, Sep. 2006, pp. 1449–1452.
[18] H. Wang, R. Lai, M. Biedenbender, G. Dow, and B. Allen, "Novel W-band monolithic push-pull power amplifiers," *IEEE J. Solid-State Circuits*, vol. 30, no. 10, pp. 1055–1061, Oct. 1995.
[19] D. Bockelman and W. Eisenstadt, "Combined differential and common-mode scattering parameters: Theory and simulation," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 7, pp. 1530–1539, Jul. 1995.
[20] Three and Four Port S-parameter Measurements. Anritsu, Application Note, pp. 1–14.
[21] J. Reed and G. J. Wheeler, "A method of analysis of symmetrical four-port networks," *IRE Trans. Microw. Theory Tech.*, pp. 246–252, Oct. 1956.
[22] E. M. T. Jones and J. T. Bolljahn, "Coupled-strip-transmission-line filters and directional couplers," *IRE Trans. Microw. Theory Tech.*, pp. 75–81, 1956.
[23] G. Vendelin, A. Pavio, and U. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990.
[24] W. E. Kock, "Metallic delay lenses," *Bell Syst. Tech. J.*, vol. 27, pp. 58–82, 1948.
[25] D. Huang, W. Hant, N. Wang, T. W. Ku, Q. Gu, R. Wong, and M.-C. F. Chang, "A 60 GHz CMOS VCO using on-chip resonator with embedded artificial dielectric for size, loss and noise reduction," in *IEEE ISSCC Dig. Tech. Papers*, 2006, pp. 1218–1227.

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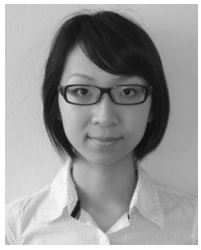
He worked for Litton/Filtronic Solid State from 1996 to 2000 as a GaAs pHEMT power and low-noise amplifier MMIC design engineer. He also designed GaAs HBT IEEE 802.11a power amplifiers for G-Plus during 2001–2003. He has been with Northrop-Grumman Aerospace Systems Sector since 2004 as a design engineer in the RF Products Department.



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Mau-Chung Frank Chang (F'96) received the Ph.D. degree from National Chiao Tung University, Taiwan. He is currently a full Professor in the Electrical Engineering Department and the Director of the High Speed Electronics Laboratory at the University of California at Los Angeles (UCLA).

Before joining UCLA, he was the Assistant Director and Department Manager of the High Speed Electronics Laboratory (1983–1997) at Rockwell Science Center, Thousand Oaks, CA. In this tenure, he successfully developed and transferred the AlGaAs/GaAs Heterojunction Bipolar Transistor (HBT) and BiFET (Planar HBT/MESFET) integrated circuit technologies from the research laboratory to the production line (now Conexant Systems and Skyworks). The HBT/BiFET productions have grown into multi-billion dollar businesses and dominated the cell phone power amplifiers and front-end module markets (exceeding 1 billion units/year). Throughout his career, his research has primarily focused on the development of high-speed semiconductor devices and integrated circuits for RF and mixed-signal communication and sensing system applications. He was the principal investigator at Rockwell in leading DARPA's ultra-high speed ADC/DAC development for direct conversion transceiver (DCT) and digital radar receivers (DRR) systems. He was the inventor of the multiband, reconfigurable RF-Interconnects, based on FDMA and CDMA multiple access algorithms, for ChipMulti-Processor (CMP) inter-core communications and inter-chip CPU-to-Memory communications. He also pioneered the development of world's first multi-gigabit/sec ADC, DAC and DDS in both GaAs HBTs and Si CMOS technologies; the first 60 GHz radio transceiver front-end based on transformer-folded-cascode (Origami) high-linearity circuit topology; and the low-phase-noise CMOS VCO (FOM < -200 dBc/Hz) with Digitally Controlled on-chip Artificial Dielectric (DiCAD). He was also the first to demonstrate CMOS oscillators in the Terahertz frequency range (324 GHz).

Dr. Chang has authored or coauthored over 270 technical papers, 10 book chapters, authored one book, edited one book and holds 20 U.S. patents. He was an editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES (1999–2001) and served as the Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 1991 and 1992, and for the *Journal of High-Speed Electronics and Systems* in 1994. He was elected to the U.S. National Academy of Engineering in 2008 for the development and commercialization of GaAs power amplifiers and integrated circuits. He was elected as a Fellow of IEEE in 1996 and received the IEEE David Sarnoff Award in 2006 for developing and commercializing HBT power amplifiers for modern wireless communication systems. He was also the recipient of the 2008 Pan Wen-Yuan Foundation Award for his fundamental contributions in developing AlGaAs/GaAs hetero-junction bipolar transistors. His recent paper "CMP Network-on-chip Overlaid with Multiband RF-Interconnect" was selected for the Best Paper Award in the 2008 IEEE International Symposium on High-Performance Computer Architecture (HPCA). He received Rockwell's Leonardo Da Vinci Award (Engineer of the Year) in 1992, National Chiao-Tung University's Distinguished Alumni Award in 1997, and National Tsing-Hua University's Distinguished Alumni Award in 2002.