A 60dB Gain and 4dB Noise Figure CMOS V-Band Receiver Based on Two-Dimensional Passive G_m-Enhancement

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***Abstract* — A direct conversion receiver which consists of low noise amplifier (LNA), mixer and programmable gain amplifier (PGA) for V-band (60GHz) applications is designed and realized in 65nm CMOS. A novel two-dimensional passive g_m-enhancement technique is devised to boost the conversion gain and lower the Noise Figure (NF) with insignificant power overhead. An overall minimum SSB NF of 3.9dB and a maximum power conversion gain of 60dB have been validated from such fabricated receiver that occupies core silicon area of 0.2mm^2 and draws 34mA from 1V supply.**

***Index Terms* — V-band, 60GHz, CMOS integrated receiver, two-dimensional g_m-enhancement, low-noise high-gain amplifier, mixer, transformer.**

I. Introduction

The 7GHz of unlicensed band around 60GHz has spurred intense research activities in low-cost, low-power and highly integrated circuits for applications in cloud computing (WiGig), ultra-high throughput WLAN (IEEE 802.11ad) and video data streaming (WirelessHD). Recent studies have indicated deep-scaled CMOS is a promising technology to reach cost-effective monolithic solution for these applications [1]. However, in order to resolve high-order modulations (i.e., 16QAM and above) for more efficient bandwidth utilization and more distant communication range, the receiver sensitivity must be raised with high gain, high linearity and low noise. Furthermore, the low noise and high linearity performance must not come at the expense of power overhead for portable systems. Consequently, a compact, low noise, high linearity and low power consumption receiver design is highly desirable. In this paper, Section II will present the proposed receiver architecture while introducing the technique of two-dimensional passive g_m-enhancement. Section III will present the tested receiver performance. Section IV will summarize the overall work.

II. Receiver Architecture

With the above considerations, we have designed and implemented a high gain, low noise and low power consumption receiver in 65nm 1P6M GP CMOS with a thick top metal of 3.4μm. As shown in Fig. 1, it is a direct-conversion receiver with an LNA tuned to 60GHz followed by a mixer to down-convert the RF signal to baseband with an external local oscillator (LO). A PGA is followed to provide programmable gains and complete the receiver chain. This prototype receiver is designed to offer high gain (up to 60dB) and low noise (<4dB) with a compact layout (0.2mm^2) and consume low current from a single 1V supply. To achieve such goals, compact and high quality factor on-chip passive devices are extensively used to boost the gain, interface between stages and facilitate biasing. To optimize the receiver gain and NF, a novel two-dimensional all passive g_m-enhancement technique is exploited to enforce 180 degree phase difference between the gate and source voltages to boost the gain without significant power penalty.

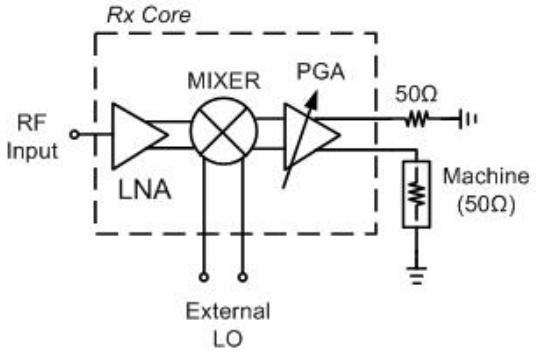

Fig. 1. V-band CMOS receiver architecture.

A. Two-Dimensional G_m-Enhanced Receiver Frontend

Fig. 2 shows the circuit schematic of a two-dimensional passive g_m-enhanced receiver frontend featuring a fully differential LNA and mixer. The first two stages of the frontend adopt differential cascode configurations for the best tradeoff in gain, noise and stability. They are followed by a transconductance stage that would convert the amplified voltage into current and magnetically couples it via a transformer into the mixer's switching-quad. At its input, the LNA employs a 1:3 transformer for various purposes of 1) matching, 2) voltage amplification, 3) single-to-differential conversion and 4) DC isolation.

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The first dimension of the two-dimensional passive g_m-enhancement is achieved by capacitor cross-coupling (C_C) between differential cascode devices. The source of one of the differential cascode devices is capacitively coupled to the gate of the other; resulting in a push-pull stretching action on the gate-source voltages (the gate bias circuitry is not shown). This effectively enhances the g_m of the differential cascode devices by a maximum factor of 2 without additional current [2].

The second dimension of the two-dimensional passive g_m-enhancement is accomplished in the form of magnetic cross-coupling of the second stage differential input devices with details explained as follows.

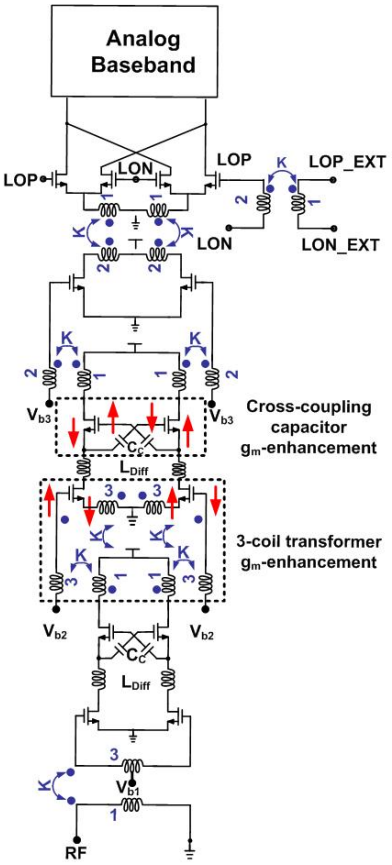

Fig. 2. Circuit schematic of the two-dimensional passive g_m-enhanced receiver frontend.

A three-coil stacking transformer (Fig.3) is interposed between the output of the first stage (at the top right) and the input of the second stage (at the bottom left). For the sake of illustration clarity, the drawn turn-ratio is chosen to be 1:1:1, whereas the actual implemented turn-ratio is 1:3:3 (one primary coil and two secondary coils). The three coils are stacked vertically on top of one another to save the area and maximize the magnetic coupling. The primary (1^{st}) coil of the transformer acts as the differential inductor load for the first stage. The 2^{nd} and 3^{rd} coils of the transformer are tied to the gates and sources of the second stage differential input devices, respectively. However, connections between sources and the 3^{rd} coil are crossed in opposite polarity from connections between gates and the 2^{nd} coil.

Due to the phase-coherence between the 2^{nd} and 3^{rd} coils and their differential implementations, such connections result in 180 degree phase stretching between induced gate-source voltages of second stage input devices. By selecting a transformer turn-ratio of 1:3:3, a maximum g_m-enhancement factor of 6 can be achieved in theory. Other magnetic g_m-enhancement techniques found in literature used two-coil transformers that lacked a degree of enhancement freedom compared with this work [3]-[4]. Moreover, the technique used in [3] was applied to a common-gate LNA that, in general, had a higher NF than a common-source LNA. To the best of our knowledge, this work represents the first attempt of g_m-enhancement by a three-coil transformer at any frequency range for the receiver design.

In addition, differential inductors, L_{Diff}, are placed between the input and cascode devices to resonate out the parasitic capacitance. The third stage of the frontend is a differential common-source transconductor that facilitates voltage-to-current conversion. A 2:1 transformer is placed between the transconductor and the double-balancing switching-quad with current amplification. A 1:2 transformer couples the LO to the switching-quad. The total current drawn by the frontend is 10mA from a 1V supply. The overall conversion gain is around 40dB at 60GHz.

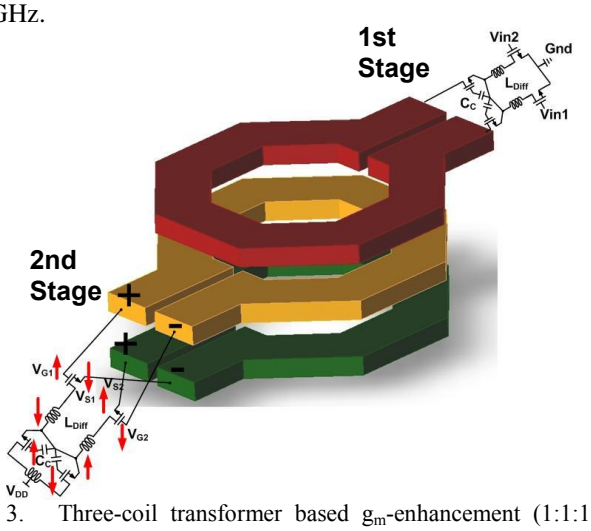

Fig. 3. Three-coil transformer based g_m-enhancement (1:1:1 turn-ratio is used for illustration purpose only; actual turn-ratio used is 1:3:3).

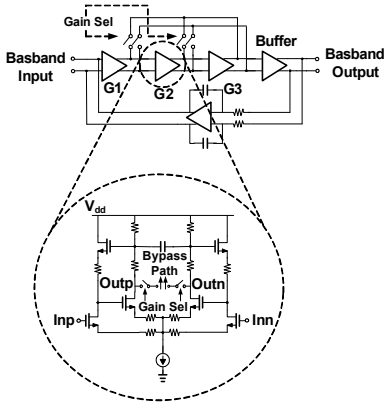

Fig. 4. Schematic of the analog baseband consists of three stages of programmable gain amplifiers.

B. Analog Baseband

Fig.4 shows the schematic of the analog baseband which consists of three stages of programmable gain amplifiers. The PGA has a maximum programmable gain of 20dB while drawing 24mW from a 1V supply. Its programmable gain is distributed among three gain stages: G1=5dB, G2=9dB and G3=6dB to optimize receiver linearity and NF. The last stage of the PGA is a buffer that drives a pair of off-chip 50ohm resistors. The buffer consumes 14mW of power which accounts for 58% of the total PGA power. However, in a fully-integrated radio, the PGA power consumption will be substantially lower because the ADC's input impedance is high. Finally, a DC-offset cancellation loop is implemented to prevent the PGA from saturating. Fig. 4 also details one of the PGA amplification stage. It is a two-stage degenerated common source amplifier with active feedback to boost the output bandwidth. We can select the PGA gain by either connecting or bypassing stages.

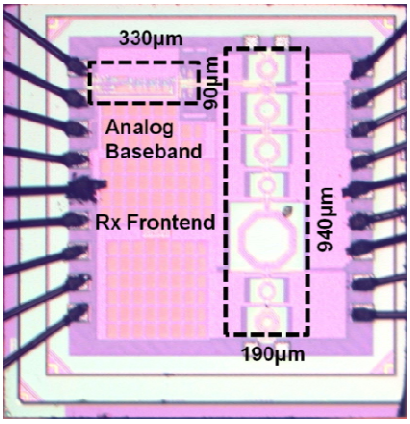

Fig. 5. Receiver die-photo.

III. Measurement Results

The receiver is fabricated in 65nm 1P6M process with the die-photo shown in Fig. 5. The receiver frontend occupies an area of 0.18mm^2 and the analog baseband occupies 0.02mm^2. Fig. 6 shows the measured power conversion gain with different gain settings versus the input frequency. The maximum gain is 60dB at 60GHz.

To qualify the effectiveness of the three-coil transformer cross-coupling in g_m-enhancement over its two-coil counterpart, an identical receiver was fabricated with the source nodes of the second stage input devices grounded and the 3rd coil floating (hereon identified as the two-coil receiver). The two receivers are then measured under identical bias conditions with the same current consumption. Fig. 7(a) and (b) compare the two receivers' gain and NF at the maximum gain setting. The three-coil transformer based receiver achieves a minimum SSB NF of 3.9dB at 59GHz. It also outperforms its two-coil counterpart in gain and NF by 8.3dB and 2.3dB at 60GHz and 59GHz, respectively.

The NF is measured using the Y-factor method. A V-band noise source (*Quinstar, QNS-FB20PV*) is inserted at the input of the receiver. The noise source is then switched on and off and the change in the output noise floor is read from the spectrum analyzer. The change in the noise floor, expressed here as $Y = N_{ON}/N_{OFF}$ and the excessive noise ratio (ENR) provided by the manufacturer can be used to find the NF = ENR/(Y-1). Careful calibration of the cable losses is required for noise de-embedding.

Fig. 8 shows the P_{out} versus P_{in} of the receiver at the lowest gain setting. The maximum output-referred 1-dB gain compression point (OP_{1dB}) is -5dbm.

The gain and noise figure variation across the spectra can be further minimized by staggering band alignments over the frequency spectrum of interest at each resonant node.

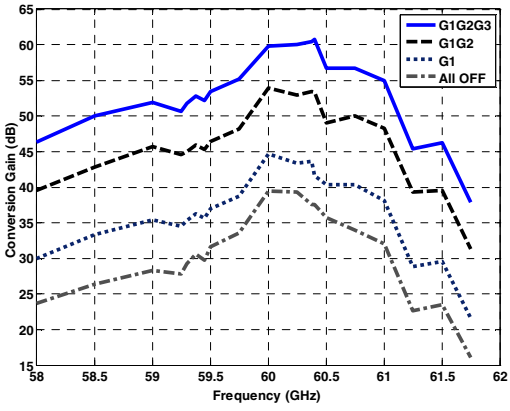

Fig. 6. Power conversion gain versus frequency for different gain settings.

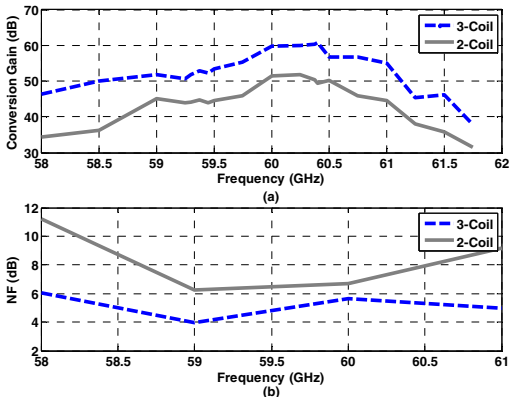

Fig. 7. (a) Comparison between 3-coil vs. 2-coil based g_m-enhancement in conversion gain; (b) comparison between 3-coil vs. 2-coil based g_m-enhancement in NF.

The power consumptions of the frontend and the analog baseband are 10mW and 24mW, respectively. Note that out of the 24mW dissipated in the analog baseband, 14mW originates from the output buffer which can be eliminated in a fully integrated radio with on-chip high input impedance ADC.

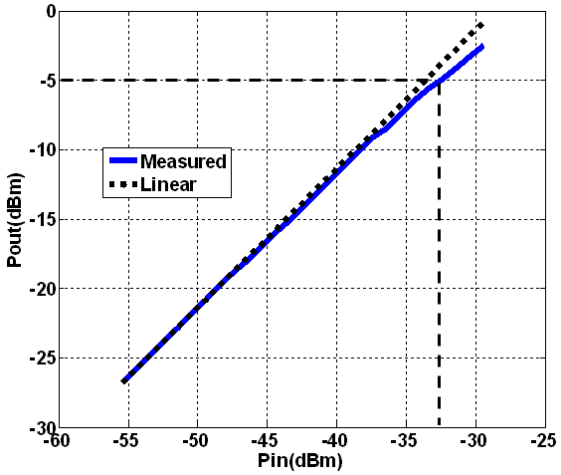

Fig. 8. P_{out} vs. P_{in} of the receiver at the lowest gain setting.

IV. Conclusion

This work realizes a V-band (60GHz) receiver with two-dimensional passive g_m-enhancement in 65nm CMOS. It demonstrates the effectiveness of a three-coil transformer based g_m-enhancement technique over prior two-coil counterparts. It achieves a minimum SSB NF of 3.9dB, maximum gain of 60dB while drawing 34mA of current from a 1V supply. Table 1 compares our receiver's performance with the state-of-the-art [1], [5], [6]. Our receiver exhibits the highest conversion gain and the lowest NF, with the smallest die area and lowest DC power consumption.

TABLE I
Comparison of State-of-the-art

	This Work	ISSCC10' [1]	RFIC10' [5]	JSSC08' [6]
Gain(dB)	**60**	35.5	18	30
NF(dB)	**3.9(SSB)**	5.6	9	7.1
Power(mW)	**34/20***	75	50	65
OP_{1dB}(dBm)	-5	N/A	N/A	0**
Supply(V)	1	1	1.8	1.2
Area(mm^2)	**0.2**	2.4***	1.2	1.4***
Process(nm)	65	65	130	90

*Excluding the power of the output buffer
**Extrapolated
***Includes on-chip LO

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