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A 7Gb/s SC-FDE/OFDM MMSE Equalizer for 60GHz Wireless Communications

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***Abstract*—This paper presents a SC-FDE/OFDM MMSE equalizer for 60GHz wireless communications in 65nm CMOS process. By applying a 4-parallel signal processing architecture, the 512pt FFT/IFFT processor, the Golay channel estimator, and the MMSE equalizer are all clocked at 1/4 input symbol sampling rate. Occupying a core area of 1.12mm^2, the symbol sampling rate at 1V supply is 1.46GS/s. With 16QAM modulation, its throughput is 5.84Gb/s while consuming 124mW in the SC-FDE mode and 88mW in the OFDM mode. With a 1.2V supply, it achieves a symbol sampling rate of 1.76GS/s with a 7Gb/s throughput while consuming 208mW in the SC-FDE mode and 148mW in the OFDM mode.**

I. Introduction

With 7GHz of unlicensed bandwidth at 60GHz, opportunities for short ranged multi-Gb/s wireless communications open up for standards such as the IEEE 802.15.3c or 802.11ad which apply both single-carrier and OFDM modulation methods [1],[2]. For high throughput wireless systems, multipath channel equalization is one of the most challenging problems in the design of a digital baseband modem. To compensate the channel induced ISI effects for these systems, OFDM modulation or time domain channel equalizers (EQ) are widely applied. An EQ applying OFDM-like 1-tap channel frequency response inversion process is preferred over time domain decision-feedback equalizers (DFEs) when communicating in a 60GHz non-line-of-sight (NLOS) multipath channel environment where the RMS channel delay spread may exceed over 10ns. In this kind of a channel environment, designing DFEs for single-carrier transmission systems requires a large number of feedback filter taps to compensate the multipath fading. In addition, the extra loop unrolling and the parallel look-ahead symbol decision hardware necessary to support multi-Gb/s throughput with complex modulations, e.g., 8PSK and 16QAM, makes DFEs impractical to apply in terms of area and power consumption. As a result, most previously reported Gb/s baseband DFEs for wireless baseband modems support only simple modulation methods like QPSK or MSK [3],[4].

From the baseband system integration point of view, when implementing a combo OFDM and single-carrier modem, it is highly desirable to have an equalization hardware architecture that would be fully utilize the FFT processor already required in the OFDM receiver to perform channel estimation, equalization, and other signal processing functions for the demodulation of single-carrier signals. Single-carrier frequency domain equalization (SC-FDE) then becomes an attractive solution as its concepts and datapath are similar to those of an OFDM receiver.

In this paper, a 7Gb/s frequency domain minimum mean squared error (MMSE) EQ chip for 60GHz wireless communication system is demonstrated. 4-parallel signal processing architecture allows this EQ chip to achieve a symbol sampling rate of 1.76GS/s while the core DSP circuits are clocked at 1/4 (1.76GHz/4= 440MHz) the input symbol rate. This EQ chip is equiped with a 512pt FFT processor and a 512pt IFFT processor to demodulate the received OFDM and single-carrier signals. It includes a time-domain Golay correlator based channel estimator to obtain the multipath channel frequency response (CFR), and it also includes a MMSE EQ for channel correction in frequency domain. To verify the proposed EQ at Gb/s throughput, differential input clock driver and low voltage differential signaling (LVDS) output drivers are also implemented in this chip.

II. Equalizer System Block Diagram

Fig. 1 shows the block diagram for 16QAM symbol equalization and the packet format of the proposed EQ system. A transmission packet starts out with Golay sequence based preambles for receiver synchronization (SYNC) followed by two 256 symbol Golay channel estimation sequences “CES a” and “CES b”. Each Golay channel estimation sequence is appended with a postfix of 128 symbols. Following the Golay sequences is the block based packet payload with cyclic prefixes (CP) in between. The length of the CP can be configured at 1/8, or 1/4 the length of a payload block and each payload block consisting of 512 samples can be demodulated with the 512pt FFT/IFFT processors.

In this proposed EQ, to process the GS/s input symbols while meeting the timing constraints of 65nm CMOS digital circuits, 4-parallel signal processing architecture is adopted. This hardware parallelism allows the core computation circuits to be clocked at 1/4 the input symbol rate. In the SC-FDE mode, after ADC processing and initial receiver synchronization, the SC-FDE takes in the 4-parallel channel distorted symbol streams and performs equalization before symbol demodulation. The equalization process is basically divided into two stages: channel estimation and channel equalization. The signal “CES_on” in Fig.1 sets the EQ in channel estimation or equalization mode. The channel estimator first applies the received Golay channel sequence correlation values to estimate the multipath channel impulse

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response (CIR) information. Next, by taking the FFT of the CIR and storing it to the SRAM, the CFR needed for frequency domain equalization can be obtained. After channel estimation, the multipath distorted symbols in the packet payload are sent to the FFT processor for equalization. In the frequency domain, these symbols are equalized based upon MMSE criterion. After channel correction, the equalized symbols are then sent to the IFFT processor for demodulation in time domain. In the OFDM mode, after initial receiver processing and channel estimation the received time domain channel distorted OFDM symbols are first sent to the frequency domain through the FFT processor. After MMSE channel equalization, the channel corrected OFDM symbols are demodulated in the frequency domain. The final 4-parallel demodulated output bit streams for both the OFDM and the SC-FDE modes are multiplexed out for post processing through the 2 on-chip LVDS output drivers.

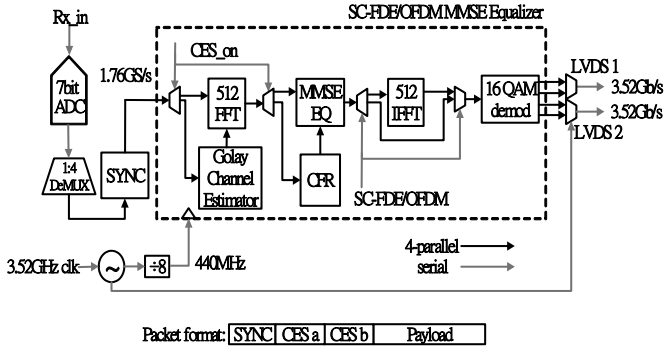

Figure1. Equalizer System Diagram

Fig. 2 shows the architecture of the 4-parallel 512pt FFT processor. It is composed of 4x time interleaved 128pt FFTs combined together through 3 complex multipliers, twiddle factor lookup tables (LUT), and a radix-4 4pt FFT unit. Each 128pt FFT processor is implemented with 7-stage pipelined radix-2 single-path delay feedback architecture. This is choosen for the 128pt FFT/IFFT processors as it has the simplest control and it can be easily extended to variable-length FFT processing for power saving purposes. With considerations of a more flexiable layout floorplan to meet the circuit timing requirements, the FIFO memories used in the FFT processors are implemented with standard cell registers.

The complex multipliers (CM) in the first 3 stages of the 128pt FFT/IFFT processors are implemented with general multipliers, while in the final 4 stages, the CM are implemented with Canonical Signed Digit (CSD) multipliers composed of hardwired shifters and adders to save area and power [5]. The 512pt FFT processor has an input of 7bits and output of 11bits while the 512pt IFFT processor has an input of 11bits and output of 8bits. Through combinations of bit truncation and numerical scaling at every stage, the 512pt FFT and IFFT processors both provide a SQNR of at least 31dB to support complex modulation methods up to 16QAM in a NLOS indoor wireless channel.

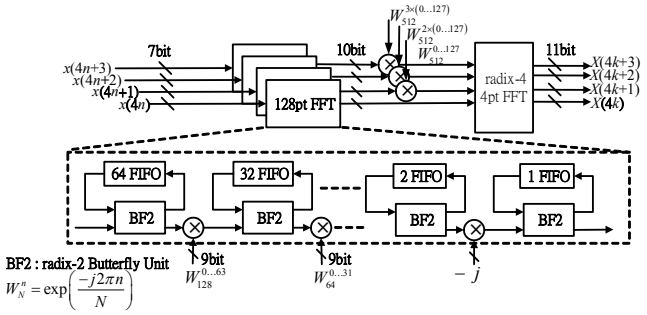

Figure 2. 512pt FFT Processor Architecture

III. CHANNEL ESTIMATOR AND MMSE EQUALIZER

The proposed channel estimator of the EQ is based on utilizing the complementary Golay sequences to obtain the CFR. Golay sequences are also applied in [1] and [2] for channel estimation. Complementary Golay sequences "CES a" and "CES b" with a length of $L=2^N$ have the property that the sum of their autocorrelation is a delta function. This property can be applied to obtain the CIR, the sum of the cross-correlation values between the received Golay sequences and the sequences themselves is the CIR. Benefits of applying Golay sequences for channel estimation are a multiplier free correlator, and a lower estimation error compared with the frequency domain based zero-forcing (ZF) method applied in [6]. In the ZF method, estimation accuracy is lost through the quantization error resulted from the estimation computation in the frequency domain where all the preamble symbols have to be first sent to the FFT processor before estimation.

Fig.3 shows the serial Golay correlator. It is very suitable for high-speed VLSI implementations since for a length $L=2^N$ Golay sequence the correlator consists of only N registers, N inverters, and $2N$ adders. In this EQ, a 4-parallel Golay correlator based channel estimator is proposed to achieve the GS/s input sampling rate. By applying a loop unrolling of 4 and architecture transformation, the functionality and the total number of delay registers in the parallel correlator remain the same compared with the serial correlator while the extra hardware for implementing the parallel correlator are the adders in each stage.

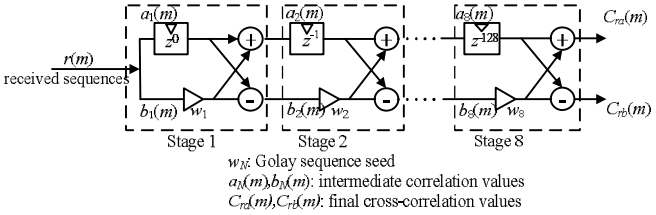

Figure 3. Serial Golay Correlator

Fig. 4 shows the 8-stage parallel Golay correlator based channel estimator. It first calculates the parallel scaled cross-correlation values $C'_{ra}(4n+j)$ and $C'_{rb}(4n+j)$, j=0~3, from the received Golay sequences. At each stage, the intermediate output correlation values are scaled down by 2 using 1bit shifters to avoid wordlength inflation in the later stages and to satisfy the Golay sequence properties. Then, $C'_{ra}(4n+j)$ and $C'_{rb}(4n+j)$ are sent to the FFT to generate frequency domain

$FC_{ra}(4k+j)$ and $FC_{rb}(4k+j)$ cross-correlation samples. The $FC_{ra}(4k+j)$ samples are first stored in the SRAM while $FC_{rb}(4k+j)$ are being computed. Once $FC_{rb}(4k+j)$ are available, each $FC_{ra}(4k+j)$ sample is read from the SRAM and the CFR is obtained by taking the average of the two at each frequency index. The final computed CFR is then written to SRAM for channel equalization.

$$\text{CFR: } H(4k+j) = (1/2)\,(FC_{ra}(4k+j) + FC_{rb}(4k+j)) \quad (1)$$

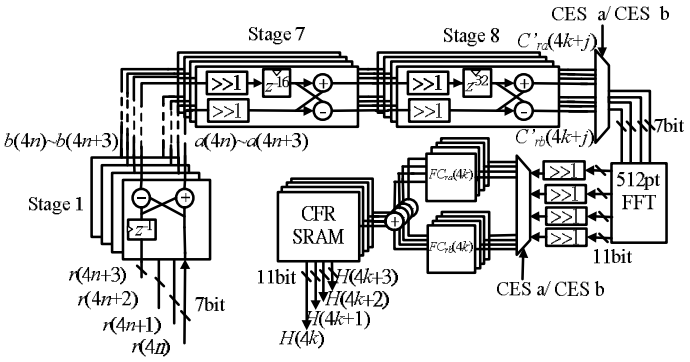

Figure 4. Parallel Golay Correlator Based Channel Estimator

Fig. 5 shows the architecture of the frequency domain MMSE EQ. The received channel distorted symbols are corrected by multiplying with the noise normalized inverse CFR coefficients [6]. In Fig. 5, SNR^{-1} is the inverse signal-to-noise ratio. To minimize the computation latency of the MMSE EQ, the divider in the EQ is implemented with a 10bit interpolated inverse value LUT and a multiplier resulting in a total latency of 2 clock cycles.

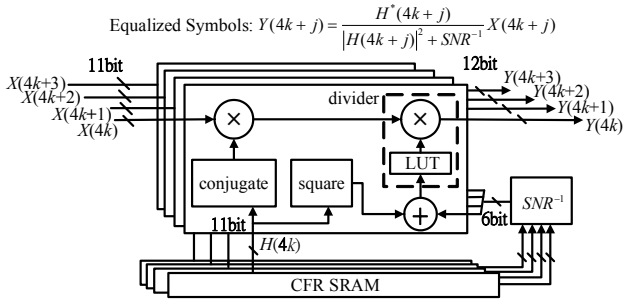

Figure 5. MMSE Equalizer Architecture

To achieve MMSE equalization, the inverse SNR value has to be estimated. One simple way to obtain the signal power estimation is to accumulate the absolute value of the estimated CFR.

$$S = (1/512)\sum_{j=0}^{3}\sum_{k=0}^{127}\left|H(4k+j)\right|^2. \quad (2)$$

The noise variance can be approximated as the accumulated squared absolute differences between the CFR and the frequency domain cross-correlation samples.

$$N = (1/2)(1/512)\left[\sum_{x=a}^{b}\sum_{j=0}^{3}\sum_{k=0}^{127}\left|H(4k+j) - FC_{Rx}(4k+j)\right|^2\right]. \quad (3)$$

The hardware necessary to compute the signal power and the noise power are basically the squaring circuits, the adders, the accumulators, and the registers. To simplify the divider to calculate the inverse of the SNR, it is implemented with LUT and a multiplier.

Fig.6 shows the uncoded BER performance curves from bit-true RTL simulation using a NLOS residential channel model with RMS delay spread of 10ns. We can see that MMSE EQs outperforms ZF EQs due to their capability of noise suppression at channel nulls. Note that in Fig.6 OFDM BER performance is more inferior compared with the performance of SC-FDE due to uncoded system assumption.

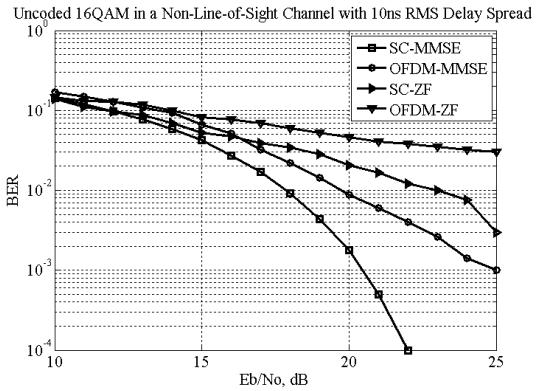

Figure 6. BER Performance Plot

IV. Implementation and Measurement Results

The SC-FDE/OFDM dual-mode baseband EQ is fabricated in TSMC 1P6M 65nm CMOS process with a core area of 1.12mm^2 and a die area of 3.22mm^2. The total gate count of the EQ chip including the test circuitry is 640K gates. On-chip BPSK, QPSK, and 16QAM (de-)modulators with 4-parallel PRBS generators and checkers are implemented to verify the EQ's functionalities. A 3-wire serial interface is installed on-chip to test different operating configurations of the EQ. Also through the 3-wire interface, test data samples can be written to the registers or the SRAM to perform EQ functional checks and the computed output samples can be read asynchronously by the PC while the EQ itself is clocked at full speed. A total of 4 clock domains are contained in this EQ chip: the high speed differential input clock, the EQ core which is clocked at 1/8 the input clock, the output multiplexiers and the LVDS output drivers which can be clocked at either the input clock or 1/2 of it depending on symbol modulation scheme, and the 3-wire interface whose sub-MHz clock is supplied from the PC. Fig. 7 shows the chip micrograph. In this chip, while all the DSP circuits are designed by digital standard cells approach, the high speed input clock driver and the LVDS output drivers are designed by an analog full custom approach.

This EQ chip has been successfully tested with a supply voltage ranging from 0.9V to 1.2V. The maximum measured symbol sampling rate at 1V supply is 1.46GS/s with 5.84Gb/s throughput when 16QAM modulation is applied. The power consumption at this configuration is 124mW for the SC-FDE mode and 88mW for the OFDM mode. The main power

difference is that the 512pt IFFT processor is turned off in the OFDM mode. When the supply voltage is increased to 1.2V, the symbol sampling rate reaches 1.76GS/s providing a throughput of 7Gb/s at a power consumption of 208mW for the SC-FDE mode and 148mW for the OFDM mode. This supports the 1.76GHz chip rate defined in the IEEE 802.15.3c standard [1]. The first part of Fig. 8 shows the measured eye diagram from one of the two LVDS output drivers when a 2.92GHz input clock is applied with 1V supply voltage in SC-FDE mode with 16QAM modulation. The second part of Fig. 8 shows the measured eye diagram when the supply voltage is increased to 1.2V and the input clock is set at 3.52GHz. The chip summary is shown in Table I. Comparison with previously reported chips having similar functions is shown in Table II.

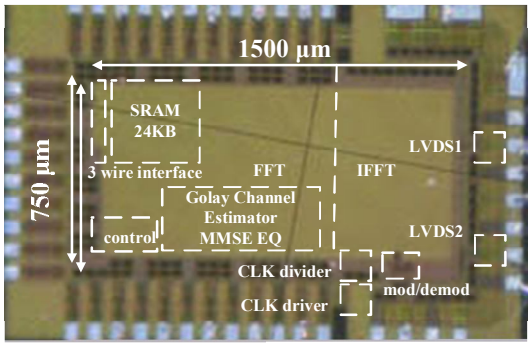

Figure 7. Equalizer Chip Micrograph

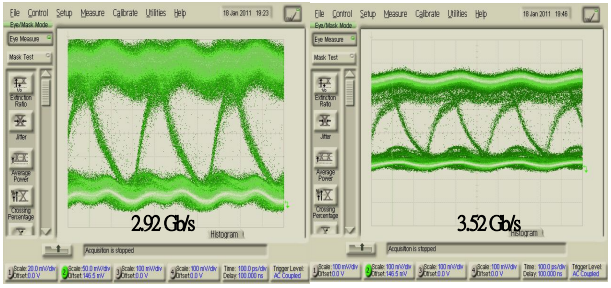

Figure 8. Measured Eye Diagrams with 16QAM modulation

TABLE I CHIP SUMMARY

Technology	TSMC 65nm CMOS
Supply	0.9V~1.2V(core), 2.5V (I/O)
Area	1.12mm^2(core), 3.22mm^2(die)
Gate Count	Total: 640K 512pt FFT: 216K 512pt IFFT: 255K Golay Channel Estimator: 76K MMSE EQ: 51k 3-Wire Serial Interface: 0.4K Others (control, testing, (de-)modulator clocking, and etc.): 42k
SRAM	24KB
Throughput	5.84Gb/s(@1.0V,365MHz) 7Gb/s(@1.2V,440MHz)
Power	SC-FDE: 124mW(@1.0V,365MHz) 208mW(@1.2V,440MHz) OFDM: 88mW(@1.0V,365MHz) 148mW(@1.2V,440MHz)

TABLE II CHIP COMPARISON

	This Work	[4]	[7]	[8]
Process	65nm	90nm	90nm	130nm
Functions	4-parallel 512-FFT/IFFT Golay MMSE EQ	DFE with 4bit-ADC	8-parallel 256 FFT	4-parallel 1024-FFT ZF EQ LDPC-OFDM
Core Area	1.12mm^2	1mm^2	3.53mm^2	17.80mm^2
Clock/Core Freq.	3.52GHz/ 440MHz	1GHz/ 1GHz	N.A./ 447MHz	N.A./ 147MHz
Gate Count	640k	N.A.	583k	1.58m
Throughput	7Gb/s (16QAM)	1Gb/s (MSK)	N.A.	820Mb/s (QPSK)
Power	208/148mW	55mW	145.5mW	391mW
Energy	29.5/21pJ/b	55pJ/b	N.A.	476pJ/b

V. CONCLUSIONS

This paper presents a SC-FDE/OFDM MMSE equalizer chip targeted for indoor 60GHz NLOS wireless communications.

By applying 4-parallel signal processing architecture, the 640K gates chip provides a 7Gb/s throughput with 16QAM modulation at 1.2V supply. To the best of our knowledge, this paper is the first to demonstrate mult-Gb/s throughput SC-FDE/OFDM MMSE equalizer with 512pt FFT and IFFT processing.

ACKNOWLEDGMENT

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