A 40-mW 7-bit 2.2-GS/s Time-Interleaved Subranging ADC for Low-Power Gigabit Wireless Communications in 65-nm CMOS

I-Ning Ku, Zhiwei Xu, Yen-Cheng Kuan, Yen-Hsiang Wang, Mau-Chung Frank Chang
Department of Electrical Engineering, University of California, Los Angeles, CA 90095, USA

***Abstract*-A 7-bit, 2.2-GS/s time-interleaved subranging CMOS ADC for low-power gigabit wireless communication system-on-a-chip (SoC) is presented. A novel time-splitting subranging architecture is invented to significantly boost the speed of individual ADC channels. In addition, a low-power and fast-settling distributed resistor array for reference voltages is proposed to mitigate mismatches within channels. The prototype is implemented in 65 nm CMOS, occupying only 0.3 mm^2 chip area and consumes 40 mW at 2.2 GS/s from a 1 V supply. Measured SNDR and SFDR are 38 dB and 46 dB, respectively, with a 1.08 GHz input at 2.2 GS/s sampling rate.**

I. Introduction

Recently, the unlicensed band around 60 GHz has stirred enormous research activities on realizing CMOS transceivers for gigabit wireless communication systems. High-speed (>1 GS/s), medium-resolution (6-8 bits) ADCs are particularly critical to achieve power-efficient, low-cost SoC solution for such applications [1-5]. Time-interleaved ADC is an ideal candidate since it is able to achieve better power efficiency by combining multiple sub-ADCs that operate at low sampling rate to generate the required high sampling rate. Time-interleaved architecture, however, suffers from channel mismatches in timing, offset, and gain among individual sub-ADCs. Moreover, as the number of channel increases, the total area increases proportionally. The routing of multiple clock phases and digital outputs becomes more intricate, and the parasitic capacitance of the long routing wire inevitably introduces a significant power penalty compared to each sub-ADC. Recent publications have shown that successive-approximation-register ADCs (SAR-ADCs) [4] and pipelined ADCs [3] are adopted as the sub-ADCs in a time-interleaved architecture. Despite its power efficiency, the sampling rate of the SAR ADC is rather limited since one clock cycle is necessary for each bit. On the other hand, the pipelined ADC can operate at a higher speed, but its high-gain op-amps are becoming more and more difficult to realize as CMOS technology continues to scale.

In this work, we invented a novel subranging ADC architecture that can offer significant higher sampling rate, and used it as the sub-ADC in the interleaved ADC. This subranging ADC-based architecture greatly reduces the required channel number so as the total chip area. Moreover, to achieve a better power efficiency, a distributed resistor array is proposed to generate reference voltages for the time-interleaved ADC. It alleviates channel gain mismatches by exploiting better matching of poly resistors, while still maintaining minimum power overhead and fast settling response.

II. Time-Interleaved Architecture and Time-Splitting Subranging ADC

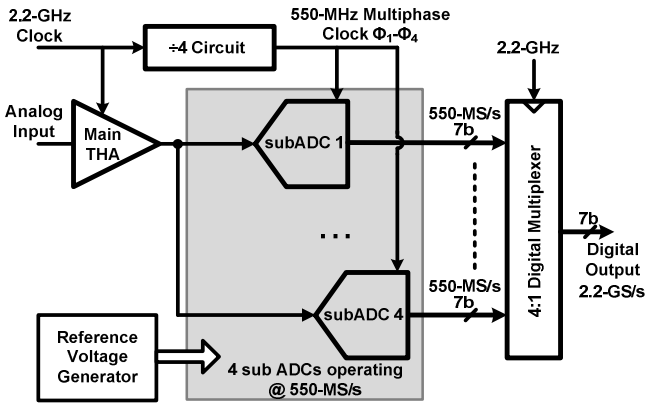

Fig. 1. Time-interleaved ADC architecture.

Fig. 1 shows the time-interleaved ADC block diagram. To minimize ADC channel number for a compact realization, high-speed 7-bit sub-ADCs with > 550 MS/s sample rate are preferred to render an interleaved ADC with four channels. Subranging architecture is suitable for such specifications due to its high sampling rate next to flash architecture, but with much smaller power and area (Fig. 2). However, conventional subranging ADC can hardly support >200 MS/s sampling rate due to tight timing budget for amplification and digital encoding, as shown in Fig. 3(a). Either extra S/H for time interleaving is required [6], which increases the total area, or extensive amount of power is consumed to boost the subranging ADC speed [7]. To overcome this limitation, we invented a time-splitting subranging architecture. Its timing diagram is shown in Fig. 3(b). The track/hold time of THA is now shifted by ¼ clock cycle. And phase 1 and phase 2 are swapped in CADC and FADC. This phase-swapping scheme results in different sampling instances. In phase 1, THA tracks and amplifies the analog input signal, while CADC amplifies the THA output concurrently. In phase 2, CADC starts the comparison and encodes the digital output for the FADC, which amplifies the signal in the subsequent phase.

978-1-4577-0223-5/11/$26.00 ©2011 IEEE

The proposed architecture has two main advantages. First, the CADC amplification and encoding time are now split into two phases instead of one. With a much more relaxed timing margin, the amplifier and comparator plus encoder now can operate separately within half clock cycle. This empowers the subranging ADC to achieve a much higher conversion rate with lower power consumption. The second advantage is that this architecture distributes the loading to sub-THA in different phases by CADC and FADC, which results in further power reduction. The cost for this architecture is a reduced tracking time. This can be compensated with a larger switch and larger clock driver that slightly increase the digital power, which only constitute a small portion of the overall power consumption. Simulation shows that the single-channel 7-bit subranging ADC running at 550 MS/s only consumes 7 mW.

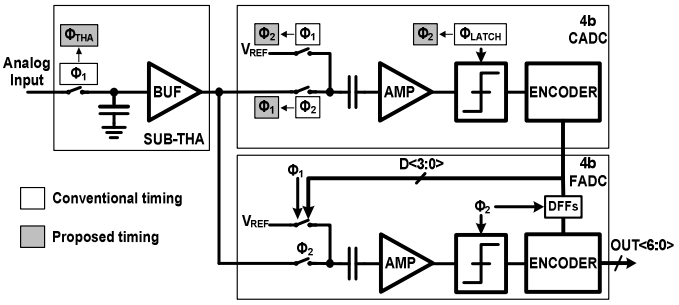

Fig. 2. Two-step subranging ADC architecture.

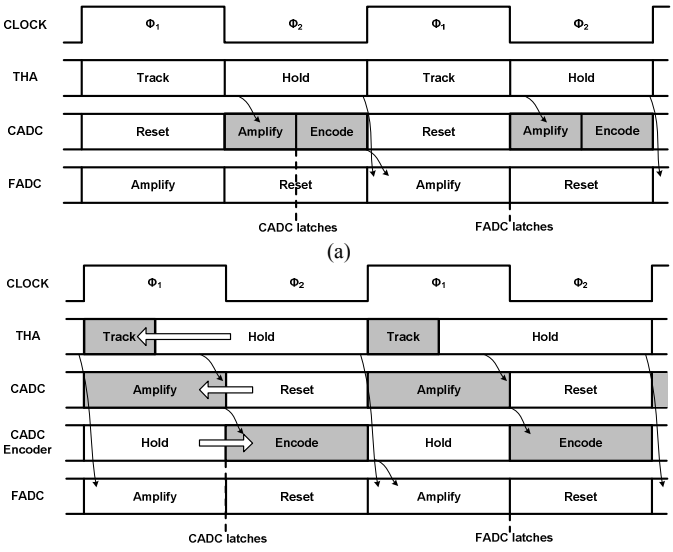

Fig. 3. (a) Conventional timing diagram. (b) Proposed time-splitting timing diagram.

III. Offset Calibration and Distributed Resistor Array Reference

Several approaches are proposed to alleviate the channel mismatches that inevitably exist in the time-interleaved ADC. A dedicated front-end track-and-hold amplifier (THA) samples the input signal at a full clock rate of 2.2 GHz to eliminate the timing mismatches among interleaved channels. The digital outputs from each sub-ADC are then multiplexed to provide a full rate 2.2 GS/s digital output. To mitigate serious offset mismatches between channels, the static offsets of each channel are calibrated out during start-up. This is done with additional corrective binary-weighted current sources inside the sub-THA buffers [8]. During calibration, sub-ADC input terminals are connected together, and the digital outputs are read out to determine the offset voltage. Then corrective current sources adjust accordingly so that offset voltage converges to zero. Since the calibration is executed offline, it consumes negligible power when the ADC is in normal operation.

Although timing mismatch and offset mismatch can be mitigated by dedicated THA and static calibration, gain mismatch still remains problematic. For sub-ADCs implemented in flash-type architecture, the main gain mismatch originates from the reference voltage mismatches. As shown in Fig. 4(a), a conventional time-interleaved ADC uses high-speed buffers to distribute reference voltages to each channel. This approach, however, has two serious drawbacks: first, the small buffer transistor, to ensure high-speed operation, generates reference voltage mismatches among interleaved channels, and therefore leads to channel gain mismatch. Second, the high-speed buffer tends to consume large power. To realize a low-power reference generator with small channel gain mismatch, we propose a distributed resistor array reference generator, as shown in Fig. 4(b). Two low-speed buffers provide reference voltages to the four parallel resistor arrays for the sub-ADCs. With N resistors in each array, resistor matching of $\Delta R/R$, and reference voltage V_{REF}, the reference voltage mismatch can be expressed as

$$\frac{\Delta V_{REF}}{V_{REF}} \approx \left(\frac{4}{(N-2)N^2} + \frac{2}{N^2} \right)^{\frac{1}{2}} \cdot \left(\frac{\Delta R}{R} \right) . \quad (1)$$

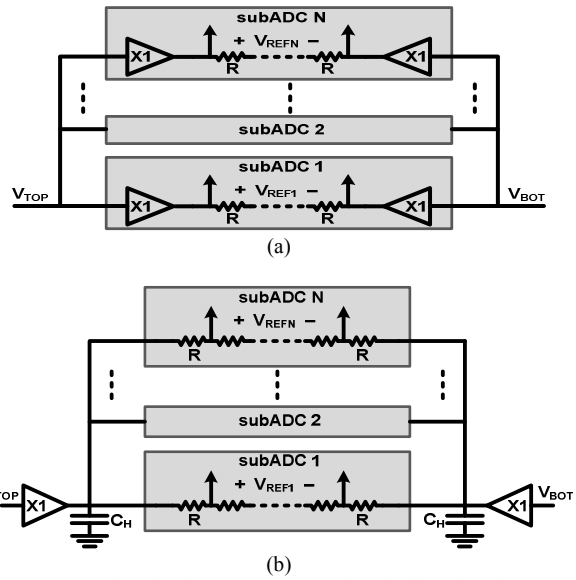

Fig. 4. (a) Conventional reference generator. (b) Distributed resistor array as reference generator.

Given N=18 and poly resistor matching $\Delta R/R$=0.85%, the reference voltage mismatch achieves an accuracy of 0.07%.

Since the resistor array can be realized with small resistor value by increasing area and introducing minor speed penalty, a fast settling higher than 1 GHz can be expected. Two additional large capacitors are applied at the buffer output to stabilize the reference voltage and reduce the kickback noise from sub-ADCs. Thereby, the proposed distributed resistor array can provide accurate multi-channel on-chip voltage references with much lower power consumption than conventional active CMOS buffer realization.

IV. Circuit Implementation

The main-THA and sub-THA are illustrated in Fig. 5. Both are open-loop pseudo-differential architecture with bootstrapped switches. NMOS source follower is used for the main-THA to operate at a higher speed of 2.2 GHz. The sub-THA consists of PMOS source follower with corrective current sources, which are in addition to the constant current bias, and used to compensate the channel offset mismatches, as mentioned in section III.

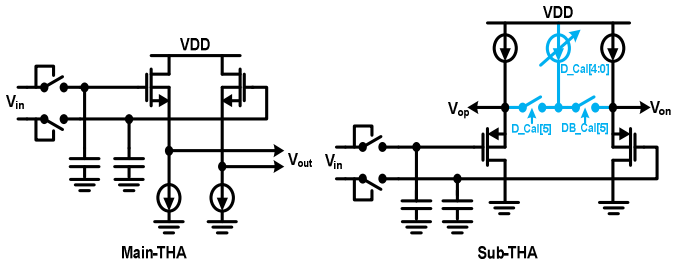

Fig. 5. Main-THA and sub-THA with corrective current sources.

Fig. 6 shows the coarse ADC (CADC) block. Since one redundant bit over-range (4 LSB) is used for digital error correction, the transistor and capacitor size can be made small once within offset and noise tolerance. The fine ADC (FADC) block is shown in Fig. 7. Two sets of binary-weighted capacitor array determine the reference level of the FADC. To achieve total 7-bit resolution, four pre-amp arrays are placed in the front of the comparator to minimize the comparator offset. 2X capacitor interpolation is employed in each pre-amp stage so that only two sets of large sampling capacitors are required to satisfy kT/C requirement, instead of fifteen sets of such capacitors. Offset storage is adopted in each stage pre-amps (Fig. 8) for DC offset cancellation. Stage 1 pre-amp uses output offset storage, since smaller sampling switch are necessary to reduce charge injection. Stage 2-4 pre-amps use input/output offset storage, which are more power efficient and support faster resetting speed.

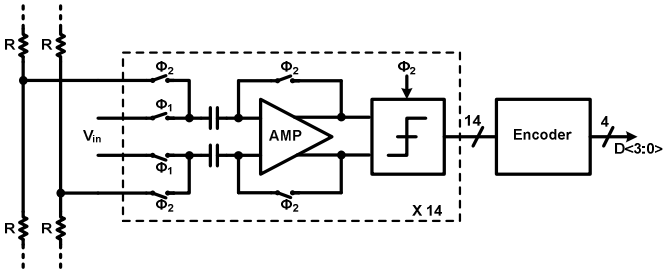

Fig. 6. 4-bit CADC block diagram.

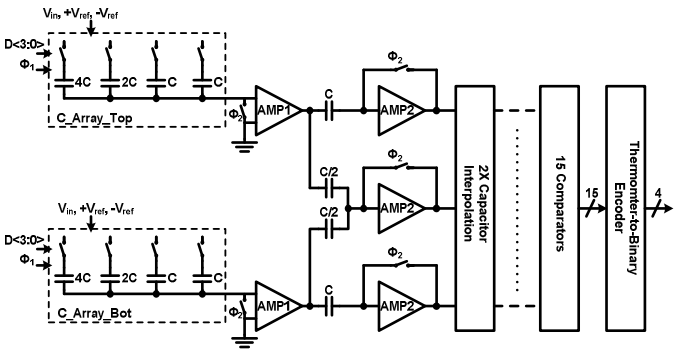

Fig. 7. 4-bit FADC block diagram.

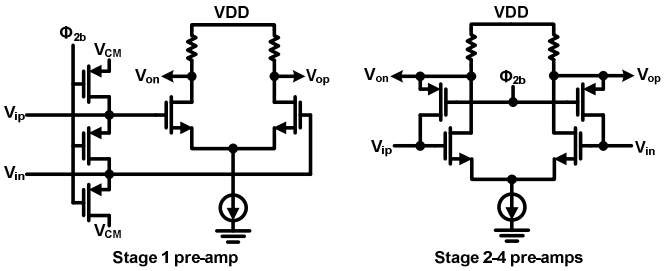

Fig. 8. FADC pre-amplifiers.

V. Experimental Results

The prototype ADC has been fabricated in 65 nm GP CMOS, and occupies 0.3 mm^2 active area, as shown in the die micrograph of Fig. 9. At 2.2 GS/s, the ADC consumes 40 mW from a 1 V supply. To characterize the ADC, the digital outputs are sampled off-chip with a decimation factor of 15. Fig. 10 shows the measured DNL and INL of the ADC, which are -0.27/0.26 and -0.68/0.53 LSB, respectively. Fig. 11 shows the measured FFT spectrum of the ADC with a 0.5 V_{pp}, 1.08 GHz input signal at 2.2 GS/s, where the SNDR and SFDR are 37.96 dB and 45.95 dB, respectively. Observed from the spectrum, the ADC performance is limited by the spurious tone caused by offset and gain mismatch as well as the 3rd harmonic. The measured offset mismatch agrees well with designed offset calibration capability; however, the spurs due to gain mismatch are larger than predicted. We suspect that this results from the gain mismatches among the sub-THA buffers. The 3rd harmonic degradation is mainly due to the THA switch bandwidth limitation, which can be improved by increasing supply voltage.

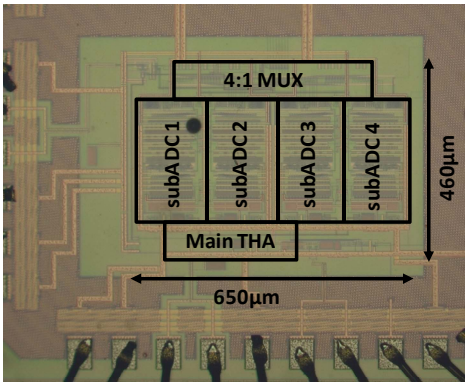

Fig. 9. Die micrograph.

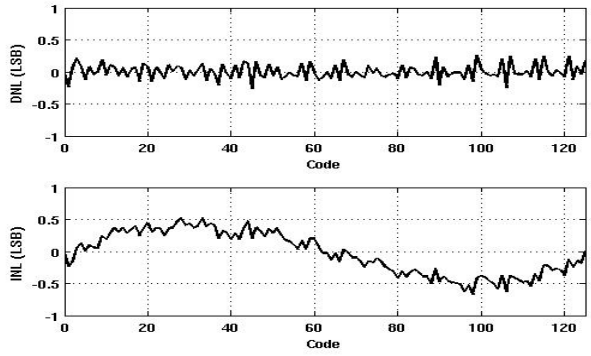

Fig. 10. Measured DNL and INL.

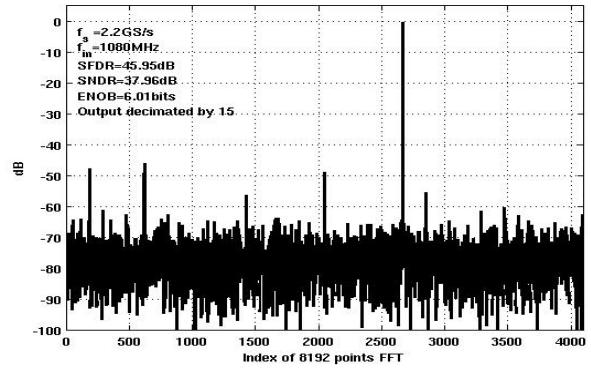

Fig. 11. Measured spectrum at 2.2 GS/s and 1.08 GHz input frequency.

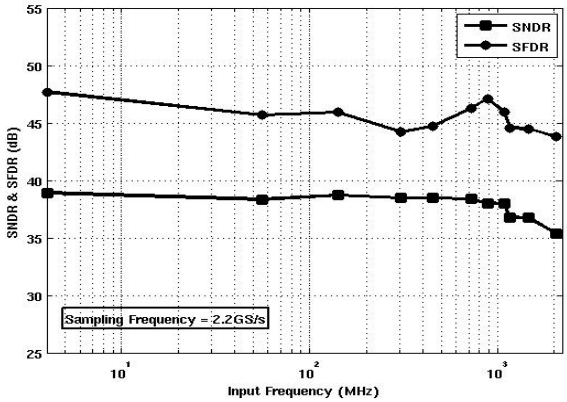

Fig. 12. Measured SNDR and SFDR vs. input frequency at f_s = 2.2 GS/s.

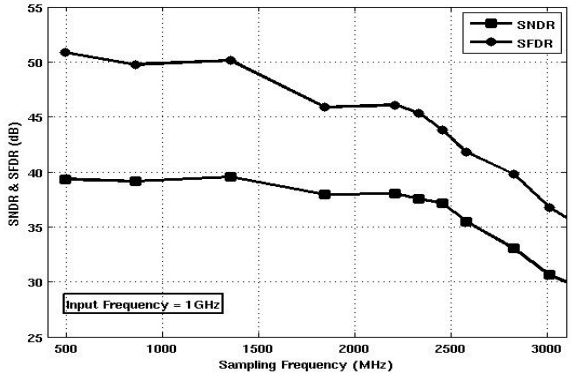

Fig. 13. Measured SNDR and SFDR vs. sampling frequency at f_{in} = 1 GHz.

Fig. 12 plots the SNDR and SFDR of the converter versus input signal frequency. At a fixed 2.2 GS/s sampling rate, the SNDR and SFDR are relatively constant and achieved an effective resolution bandwidth (ERBW) of 1.8 GHz. Fig. 13 plots the SNDR and SFDR of the converter versus sampling frequency with a fixed input frequency of 1 GHz. The ADC also demonstrates an ENOB > 5.5 bits at 2.6 GS/s. The prototype ADC achieves a figure of merit (F.O.M.) of 0.28 pJ/conv.-step, which is defined as

$$F.O.M. = \frac{power}{\min(f_s, 2ERBW) \cdot 2^{ENOB, \min(f_s/2, ERBW)}} \quad . \qquad (2)$$

Table I shows the performance summary of the ADC and its comparison to the state-of-the-art ADCs with 7-8 bits resolution and >1 GS/s sampling rate. To the authors' best knowledge, this ADC achieves the best F.O.M. and smallest active area in this category. This ADC has also been successfully integrated into a 60 GHz wireless transceiver for gigabit wireless applications.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[5]	[4]	[3]
Process	**65nm**	65nm	45nm	90nm
Resolution (bit)	**7**	8	7	7
Sampling Rate (GS/s)	**2.2**	1.5	2.5	1.1
Supply (V)	**1.0**	1.0	1.1	1.3
ENOB @ Nyquist (bit)	**6.0**	5.7	5.4	5.7
Power (mW)	**40**	35	50	92
FOM (pJ/conv.-step)	**0.28**	0.42	0.48	1.18
Active Area (mm^2)	**0.3**	0.5	1	0.37

ACKNOWLEDGMENTS

The work is supported in part by DARPA.

REFERENCES

[1] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.6mW 6b 2.2GS/s 4-times Interleaved Fully Dynamic Pipelined ADC in 40nm Digital CMOS," *ISSCC Dig. Tech. Papers,* pp. 296-297, Feb. 2010.

[2] Y. Nakajima et al., "A Background Self-Calibrated 6b 2.7 GS/s ADC With Cascade-Calibrated Folding-Interpolating Architecture," *IEEE J. Solid-State Circuits,* vol. 45, no.4, pp. 707-718, April 2010.

[3] C.C. Hsu et al., "A 7b 1.1GS/s Reconfigurable Time-Interleaved ADC in 90nm CMOS," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 66-67, June 2007.

[4] E. Alpman, H. Lakdawala, L.R. Carley, and K. Soumyanath, "A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital CMOS," *ISSCC Dig. Tech. Papers,* pp. 76-77, Feb. 2009.

[5] J. Proesel, G. Keskin, J.-O. Plouchart, and L. Pileggi, "An 8-bit 1.5GS/s Flash ADC Using Post-Manufacturing Statistical Selection," *Proc. CICC,* Sep. 2010.

[6] Z. Cao and S. Yan, "A 52mW 10b 210MS/s Two-Step ADC for Digital-IF Receivers in 0.13μm CMOS," *Proc. CICC,* pp. 309-312, Sep. 2008.

[7] K. Ohhata, K. Uchino, Y. Shimizu, K. Oyama, and K. Yamashita, "Design of a 770-MHz, 70-mW, 8-bit Subranging ADC Using Reference Voltage Precharging Architecture," *IEEE J. Solid-State Circuits,* vol. 44, no.11, pp. 2881-2890, Nov. 2009.

[8] H. Yu and M.-C.F. Chang, "A 1-V 1.25-GS/S 8-Bit Self-Calibrated Flash ADC in 90-nm Digital CMOS," *IEEE Trans. Circuits and Systems II,* vol. 55, no.7, pp. 668-672, July 2008.