Compact low-power 7-bit 2.6 GS/s 65 nm CMOS ADC for 60 GHz applications

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A 7-bit, 2.6 GS/s time-interleaved analogue-to-digital converter (ADC) for 60 GHz applications is designed and fabricated in 65 nm CMOS. The proposed subranging ADC architecture with time-shifting track-and-hold and two-phase amplification and encoding significantly enhances the speed of individual ADCs and reduces the number of interleaved channels to only four. At 2.6 GS/s sampling rate with a 1.355 GHz input signal, the ADC achieves an effective number of bits of 5.5 bits. Its core occupies 0.3 mm^2 chip area and draws 45 mA current from a 1 V supply.

Introduction: High-speed (>1 GS/s), medium resolution (6–8 bits) analogue-to-digital converters (ADCs) with low power consumption and small area are key to 60 GHz CMOS transceivers for high data rate wireless communications. Time-interleaved (TI) ADC architecture, which combines multiple low-speed power-efficient subADCs, is considered an ideal candidate to achieve such specifications and is widely employed in recent developments [1, 2]. The time-interleaved ADC, however, suffers from several drawbacks such as large area as the number of channels increases to achieve a high aggregated sampling rate, complicated signal routing, and excessive parasitic of long routing lines that degrade circuit speed. Moreover, significant mismatches among channels can deteriorate ADC linearity performance. All these necessitate circuit design techniques that can reduce the number of interleaved channels and minimise area and power overheads.

In this reported work, we designed and implemented a time-interleaved ADC in 65 nm general purpose (GP) CMOS. A novel subranging ADC architecture with significantly higher sampling rate is proposed and serves as the core of each subADC in the time-interleaved ADC. This subranging-based architecture greatly reduces the required channel number while maintaining low power consumption. It results in an ADC with optimum performance in terms of total area and power efficiency compared to the successive-approximation-register (SAR) based [1] or pipelined-based [2] time-interleaved ADCs. In addition, it has been successfully integrated into a 60 GHz CMOS transceiver.

Circuit architecture: Fig. 1 shows the architecture of this 7-bit, 2.6 GS/s time-interleaved ADC. It consists of a dedicated front-end track-and-hold amplifier (THA) that samples the input signal at 2.6 GHz clock rate, and is followed by four subranging ADCs, all of which operate at 650 MS/s. The front-end THA, which comprises an open-loop switch-cap circuit and an NMOS source follower, serves the purpose of removing the channel timing mismatch induced by the unequal input delay and clock skew. The subsequent four subranging ADCs sub-sample and hold the output signal of the THA at 650 MHz clock rate in four different phases and quantise it. The digital outputs are then multiplexed to generate a full-rate 2.6 GS/s output.

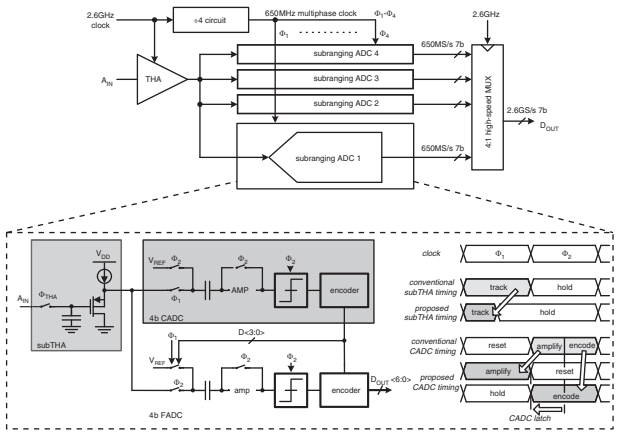

Fig. 1 *Architecture of 7-bit 2.6 GS/s time-interleaved ADC*

In each subADC, a two-step subranging architecture is adopted because of its excellent power efficiency in medium resolution and high-speed ADCs [3–5]. However, as shown in Fig. 1, conventional subranging ADCs hardly exceed 300 MS/s since the coarse ADC is required to perform amplification, comparison, and encoding in a limited time. To achieve high-speed operation, either extra interleaving channels need to be implemented [3], or an excessive amount of current is required to boost the ADC speed [4] in conventional approaches. Here, we propose a new two-step subranging ADC architecture. It consists of a subTHA, a 4-bit coarse ADC (CADC), and a 4-bit fine ADC (FADC) to achieve overall 7-bit resolution with 1-bit redundancy. Different from the conventional subranging architecture, the tracking time of the subTHA is shifted by a quarter clock cycle while the CADC and the FADC operate in different sampling instances. As shown from the timing diagram in Fig. 1, the amplification and encoding are now operated in two adjacent phases instead of one. This enables the subranging ADC to operate at a higher sampling rate and with lower power consumption through a much more relaxed timing margin. Moreover, it further reduces the capacitive load imposed to the subTHA since the CADC and the FADC sample the subTHA output at different phases. This load-reduction results in more power saving. Simulation shows that each subranging ADC consumes only 8 mW at 650 MS/s.

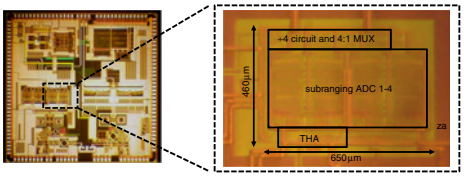

Fig. 2 *Die photo of ADC integrated in 60 GHz transceiver*

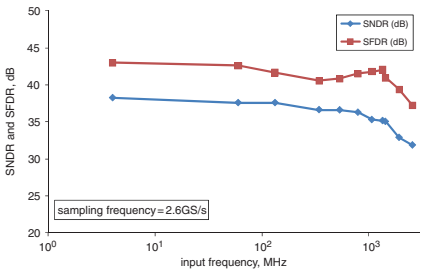

Fig. 3 *Measured performances against input frequency at 2.6 GS/s*

Table 1: Performance summary and comparison with prior arts

	This work	ISSCC09 [1]	VLSI07 [2]
Resolution (bit)	7	7	7
Sampling rate (GS/s)	2.6	2.5	1.1
Supply (V)	1.0	1.1	1.3
Power (mW)	45	50	92
ENOB at Nyquist (bit)	5.5	5.4	5.7
FOM (pJ/conv.-step)	**0.38**	0.48	1.18
Active area (mm^2)	**0.3**	1	0.37
Architecture	TI + subranging	TI + SAR	TI + pipelined
Technology	65 nm	45 nm	90 nm

Measurement results: The time-interleaved ADC prototype has been fabricated in TSMC 65 nm 1P6M CMOS process. Fig. 2 shows the die micrograph of the ADC integrated in a 60 GHz transceiver, in which the ADC occupies 0.3 mm^2 active chip area. At 2.6 GS/s sampling rate, the ADC consumes 45 mW from a 1 V supply. To characterise the ADC, digital outputs are sampled off-chip with a decimation factor of 15 and stored in the logic analyser. The measured DNL and INL are −0.25/0.25 and −0.74/0.87 LSB, respectively. Fig. 3 shows the measured SNDR and SFDR of the ADC against input frequency at 2.6 GS/s. At Nyquist rate for 1.355 GHz input frequency, measured SNDR and SFDR are 35.15 and 42.03 dB, respectively. The effective number of bits (ENOB) is 5.5 bits. According to Fig. 3, the effective resolution bandwidth (ERBW) is around 1.4 GHz. The degradation of SNDR and SFDR after 1.4 GHz is primarily due to the limited bandwidth of the front-end THA. This ADC achieves a figure-of-merit (FOM) of 0.38 pJ/conv.-step, which is defined by the equation: FOM = power/(min(f_s,2ERBW) × 2ENOB). Table 1 summarises the performance and its comparison to other state-of-the-art ADCs with

7-bit resolution and >1 GS/s sampling rate. To our best knowledge, this ADC demonstrates the best FOM and the smallest active area in this category.

Conclusion: This work realised a 7-bit, 2.6 GS/s time-interleaved ADC in 65 nm CMOS with an ENOB of 5.5 bits at Nyquist rate and power consumption of 45 mW under a 1 V supply. Utilising the proposed sub-ranging ADC as each subADC, the time-interleaved ADC achieves a state-of-the-art FOM of 0.38 pJ/conv.-step and occupies only 0.3 mm^2 active area. The outstanding power efficiency and compact area of this ADC validates our proposed architecture and demonstrates its potential to be a cost-effective and low-power building block for 60 GHz wireless applications.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Alpman, E., Lakdawala, H., Carley, L.R., and Soumyanath, K.: 'A 1.1 V 50 mW 2.5 GS/s 7b time-interleaved C-2C SAR ADC in 45 nm LP digital CMOS'. ISSCC, Grenoble, France, 2009, pp. 76–77
2 Hsu, C.C., Huang, C.C., Lin, Y.H., Lee, C.C., Soe, Z., Aytur, T., and Yan, R.H.: 'A 7b 1.1GS/s reconfigurable time-interleaved ADC in 90 nm CMOS'. IEEE Symp. on VLSI Circuits, Kyoto, Japan, 2007, pp. 66–67
3 Figueiredo, P.M., Cardoso, P., Lopes, A., Fachada, C., Hamanishi, N., Tanabe, K., and Vital, J.: 'A 90 nm CMOS 1.2 V 6 b 1 GS/s two-step subranging ADC'. ISSCC, San Francisco, CA, USA, 2006, pp. 2320–2329
4 Ohhata, K., Uchino, K., Shimizu, Y., Oyama, K., and Yamashita, K.: 'Design of a 770-MHz, 70-mW, 8-bit subranging ADC using reference voltage precharging architecture', *IEEE J. Solid-State Circuits*, 2009, **44**, (11), pp. 2881–2890
5 Shimizu, Y., Murayama, S., Kudoh, K., and Yatsuda, H.: 'A split-load interpolation-amplifier-array 300 MS/s 8b subranging ADC in 90 nm CMOS'. ISSCC, Grenoble, France, 2008, pp. 552–553