28.1 An 8.4Gb/s 2.5pJ/b Mobile Memory I/O Interface Using Simultaneous Bidirectional Dual (Base+RF) Band Signaling

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Power and bandwidth requirements have become more stringent for DRAMs in recent years. This is largely because mobile devices (such as smart phones) are more intensively relying on the use of graphics. Current DDR memory I/Os operate at 5Gb/s with a power efficiency of 17.4mW/Gb/s (i.e., 17.4pJ/b)[1], and graphic DRAM I/Os operate at 7Gb/s/pin [3] with a power efficiency worse than that of DDR. High-speed serial links [5], with a better power efficiency of ~1mW/Gb/s, would be favored for mobile memory I/O interface. However, serial links typically require long initialization time (~1000 clock cycles), and do not meet mobile DRAM I/O requirements for fast switching between active, standby, self-refresh and power-down operation modes [4]. Also, traditional baseband-only (or BB-only) signaling tends to consume power super-linearly [4] for extended bandwidth due to the need of power hungry pre-emphasis, and equalization circuits.

To overcome aforementioned technical limitations, we propose to implement a Dual (Base+RF) Band Interconnect (DBI) to enable high throughput data rate and low power operation in a mobile DRAM I/O interface. Unlike the conventional BB-only signaling, the proposed DBI signaling, as shown in Fig. 28.1.1, uses both BB and RF bands for simultaneous dual data stream communications, but shares the common transmission line (T-Line). Instead of limiting the baseband operation within its linear-power-consumption region versus the bandwidth, we can now double the interface bandwidth by using DBI and still maintain the linear-power-consumption versus the bandwidth in each of the dual bands. Additionally with forwarded clocking that adds a small overhead to DRAM I/O (Fig. 28.1.1), the DBI enables simultaneous bidirectional data links [6] as well. By applying such links to DRAM I/O data (DQ) and command/address (C/A), we can greatly reduce the DRAM access time by requesting DRAM read/write-operations simultaneously. Consequently, we can implement bidirectional DRAM I/Os with a much higher aggregate data rate (up to 10Gb/s) and lower power operation (2.5mW/Gb/s).

Figure 28.1.2 shows the DBI transceiver schematic of the memory controller side with an RF-band transmitter (RFTX) and a baseband receiver (BBRX). The RFTX contains an LC tank VCO, an amplitude-shift keying (ASK) modulator and a frequency-selective transformer. In RFTX, the VCO first generates RF carrier at 23GHz and continuously modulates M1 and M2 for ASK communication. The data stream $D_{1(RF)}$ modulates the 23GHz carrier by switching on/off the current flow through M3 and M4 to complete the ASK modulation. The modulated output is then inductively coupled into an off-chip T-Line by way of an on-chip differential transformer. The BBRX amplifies the incoming data stream $D_{2(BB)}$ using buffers with On-Die Termination (ODT) to set the common mode voltage at the transformer center tap and remove the impedance mismatch. As a result, we transmit and receive $D_{1(RF)}$ and $D_{2(BB)}$ data streams concurrently under both differential (RF-band) and common (BB) modes. While DBI's dual band streams are simultaneously transmitted and received, the inter-band interference can be suppressed by spectra separation and the orthogonal property between the differential and common mode signaling.

Figure 28.1.3 shows the DBI transceiver of the DRAM side with a RF-band receiver (RFRX) and a baseband transmitter (BBTX). The RFRX first splits data streams into the BB and RF-band by using an on-chip frequency-selective transformer. The band-pass filtered RF-band data stream is then injected to the receiver differential mutual-mixer with differential input signals and down-converted to the baseband data $D_{1(RF)}$. The termination voltage and the tail source current determine the operating point of the mixer. We utilize a pair of resistor loaded switching devices and a class-AB amplifier with resistive feedback to further filter out the residue of the RF carrier with a 12.7dB gain. By taking both active device and passive component parasitic into account, we can design the mixer with high signal integrity and high immunity to supply noise without extensive phase/frequency synchronization circuit. The BBTX utilizes a low common-mode push-pull output driver with Off-Chip Driver (OCD) based on digital impedance control logic to evade impedance mismatch and reduce sensitivity to PVT variations. In the meantime, the BB output driver couples the data stream $D_{2(BB)}$via the common mode (i.e. the center tap of the differential transformer) to the off-chip T-Line.

Since the RF-band in our proposed DBI can easily use a high microwave frequency carrier to minimize the inter-band interference (in this case 23GHz), its signal bandwidth to carrier ratio becomes relatively small so that equalization is generally unnecessary. This dual (BB+RF) band concept can further extended to Base+Multiple-RF bands in the future, such that multiple data streams can be simultaneously transmitted through a shared memory I/O interface T-Line, as long as a multi-band coupling scheme can be devised. Furthermore, since the receiver mixer with differential input signals only senses the incoming signal's amplitude, the frequency and phase synchronizations between RF TX and RX are not required. This greatly simplifies the overall memory I/O interface design. For the same reason, the BER is also expected to be better than that of phase sensitive modulation schemes.

The measured waveforms for DBI input and recovered data streams, and the frequency spectrum of the RF carrier at 23GHz are depicted in Fig. 28.1.4. Figure 28.1.5 shows measured eye diagrams of aggregate 8.4Gb/s (4.6Gb/s BB + 3.8Gb/s RF-band) data throughput over a 10cm T-Line on a FR4 board and 10Gb/s (5Gb/s BB + 5Gb/s RF-band) over the same distance T-Line on a Roger 4003C board, respectively. Both are with <14ps jitter performance.

In summary, we have designed and fabricated a DBI for mobile DRAM I/O interface in 65nm CMOS to obtain an aggregate data throughput of 8.4Gb/s and 10Gb/s on FR4 and Roger test boards, respectively, with power consumptions of 21mW and 25mW. The BERs for both test boards are measured as $<1\times10^{-15}$ by using 2^{23}-1 PRBS from the Agilent-70843C. Figure 28.1.6 compares the DBI performance to that of prior memory I/O interfaces. Among all, the DBI exhibits the highest aggregate data throughput, best energy efficiency (~2.5pJ/b) and smallest active die area (0.14mm^2 with die photo shown in Fig. 28.1.7).

References:

[1] Kwang-Il Oh, et al., "A 5-Gb/s/pin Transceiver for DDR Memory Interface with a Crosstalk Suppression Scheme," *IEEE J. Solid-State Circuits*, vol. 44, pp. 2222-2232, Aug. 2009.

[2] Kyung-Soo Ha, et al., "A 6Gb/s/pin Pseudo-Differential Signaling Using Common-Mode Noise Rejection Techniques Without Reference Signal for DRAM Interfaces," *ISSCC Dig. Tech. Papers*, pp.138-139, Feb. 2009.

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[6] Jae-Kwan Kim, et al., "A 3.6 Gb/s/pin simultaneous bidirectional (SBD) I/O interface for high-speed DRAM," *ISSCC Dig. Tech. Papers*, pp.414-415, Feb. 2004.

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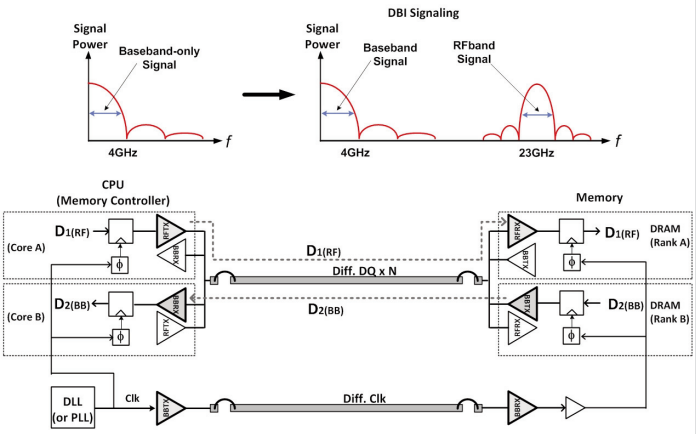

Figure 28.1.1: DBI-based mobile memory I/O interface with forwarded-clock for simultaneous bidirectional signaling.

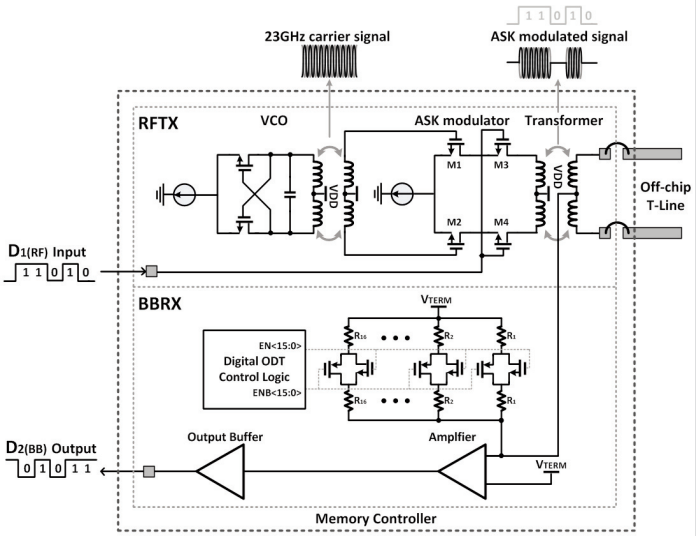

Figure 28.1.2: DBI transceiver schematic of the memory controller side.

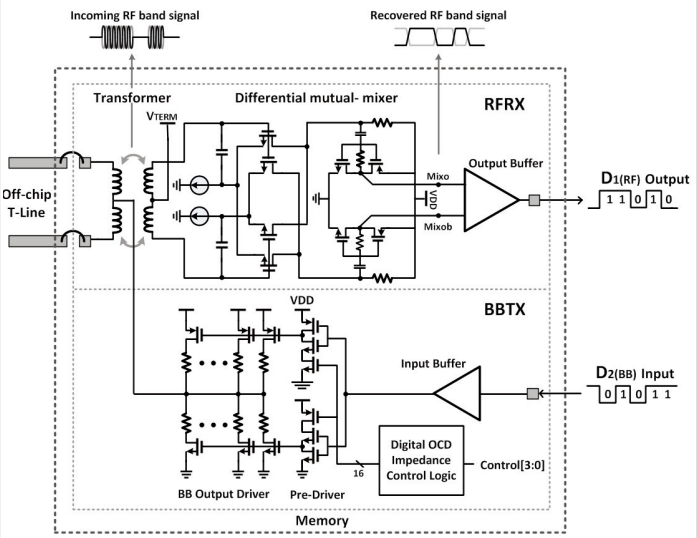

Figure 28.1.3: DBI transceiver schematic of the memory side.

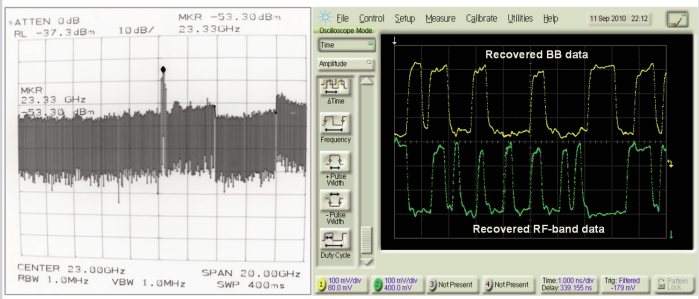

Figure 28.1.4: Measured 23.3GHz RF-band carrier and simultaneous bidirectional 8.4Gb/s Dual (Base+RF)-band waveforms.

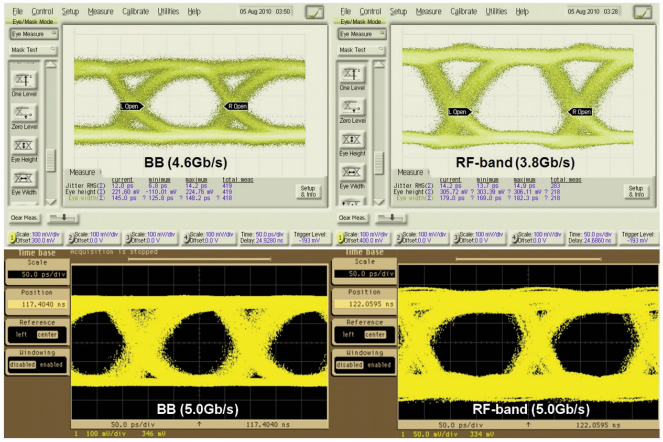

Figure 28.1.5: Measured eye diagrams of aggregate 8.4Gb/s (4.6Gb/s BB + 3.8Gb/s RF-band) and 10Gb/s (5Gb/s BB + 5Gb/s RF-band) data rate, respectively, on FR4 and Roger 4003C test boards.

	[1] JSSC 2009	[2] ISSCC 2009	[4] JSSC 2010	This Work	
				FR4 DBI	Roger DBI
Technology	0.18µm CMOS	0.13µm CMOS	40nm CMOS	65nm CMOS	65nm CMOS
Bands	BB	BB	BB	BB+RF(23GHz)	BB+RF(23GHz)
Supply	1.8V	1.2V	1.1V	1.0V	1.0V
T-Line Length	10cm (FR4)	5cm (N/A)	7cm (FR4)	10cm (FR4)	10cm (Roger)
Aggregate data rate	(BB-only) 5Gb/s	(BB-only) 6.0Gbps	(BB-only) 4.3Gbps	(RF+BB) 8.4Gb/s	(RF+BB) 10Gb/s
Communication	Bidirectional	Bidirectional	Bidirectional	Simultaneous bidirectional	Simultaneous bidirectional
Energy per bit	17.4pJ/bit	15.8pJ/bit	3.3pJ/bit	2.5pJ/bit	2.5pJ/bit
Total power	87mW	95mW	14.4mW	11mW (BB) 10mW (RF)	13mW (BB) 12mW (RF)
Chip Area	0.52mm^2	0.30mm^2	N/A	0.14mm^2	0.14mm^2
Measured BER	10^{-12} (PRBS2^{15}-1)	10^{-12} (PRBS2^{15}-1)	N/A	$<10^{-15}$ (PRBS2^{23}-1)	$<10^{-15}$ (PRBS2^{23}-1)

Figure 28.1.6: DBI performance summary and comparison with prior arts.

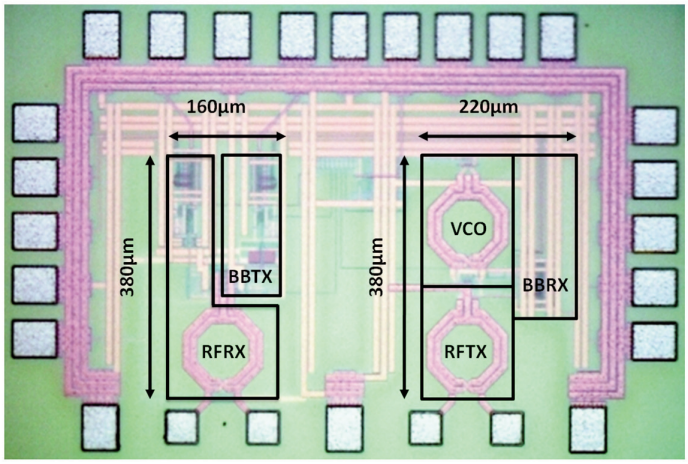

Figure 28.1.7: Die Photo of DBI transceiver.

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