D-Band Frequency Synthesis Using a U-band PLL and Frequency Tripler in 65nm CMOS Technology

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***Abstract* — This paper presents a digitally controlled frequency synthesizer in 65nm CMOS technology for D-band transceiver applications. The synthesizer uses a low frequency U Band (44-48 GHz) phase-locked loop to track a 50 MHz reference and then employs an injection locked frequency tripler (ILFT) to provide output that can be tuned between 130 and 133 GHz. The proposed D-band synthesizer offers a directly measured phase noise of –82.5 dBc/Hz at 1 MHz offset from the carrier and consumes 92mW of power. The entire syntheszier occupies 0.68mm^2 of silicon area.**

I. INTRODUCTION

D-band mm-wave radio transceiver systems are beginning to emerge for applications including Gb/s rate communications, biomedical sensing, mm-wave imaging and radar applications. [1.2.3] Since all of these applications require large bandwidth, providing a low phase noise local-oscillator (LO) signal becomes critical as the integrated jitter will quickly accumulate when intregrated over such wide channels. Traditionally frequency synthesis at frequencies beyond 100 GHz has been dominated by III-V technology such as InP and GaAs HBT. While these technologies provide solutions for generation of such high frequency carriers with execellent phase noise performance, they are typically quite power hungry and offer limited integration with digital ASIC, data converters, and other necessary mm-wave transceiver components.

Recent advances in the RF performance of deep-sub-micron CMOS technology have enabled the possibility of generating these high frequency carriers in silicon technology while still retaining phase noise suitable for wideband communications. For example [4] presents a high performance W-band PLL operating in a 180nm BiCMOS technology and still delivering –92 dBc/Hz of phase noise at a 1MHz offset.

The U-Band (42-48) GHz PLL previously presented in [2] uses an injection locked divider and injection locked output buffer in conjunction with a current-mode logic (CML) programmable frequency divider. Tuning for the divider, injection locked buffer and primary VCO are controlled by digitally controlled artifical dielectric (DiCAD) elements [2]. While this architecture delivers excellent performance at 42-48 GHz it becomes problematic as the frequency is increased up to D-band since the maximum input frequency of the CML based programmable divider is limited to 25 GHz at most.

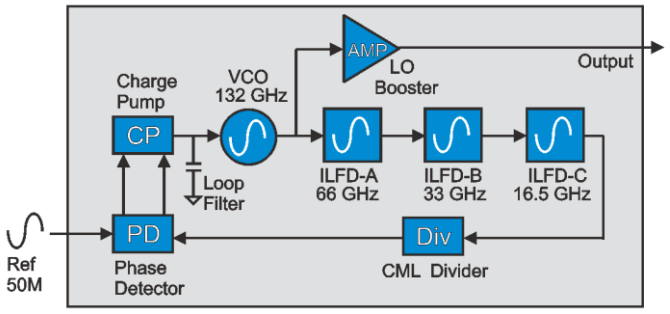

Fig. 1 A cascaded divider PLL for D-band requiring 3 different injection locked dividers (A,B,C) in cascade to provide a low enough frequency input to the CML programmable divider.

As shown in Fig 1, Using a regular cascade of injection locked frequency dividers (ILFDs) for D-band would require at least three ILFD stages to divide the 132 GHz carrier signal down to a frequency that the current-mode logic can accept (16 GHz). Such a high count of slave oscillators could potentially limit the tuning range of the synthesizer and ensuring that the frequency alignment was sufficient to maintain the locked condition would also create difficulty. The large process variation associated with deep-sub-micron CMOS technology will futher exasterbate the frequency alignment. An additional difficulty is that varactors provide very low-Q beyond 100 GHz causing a considerable reduction in oscillator swing and potentially creating difficulties in achiving startup. For this reason high frequency oscillators beyond W-band (110 GHz) typically offer very narrow tuning ranges of only 1-2%. With the narrow tuning ranges involved, correctly aligning all 3 slave oscillators at design becomes even more difficult and the challenges of process variation are further inflated.

II. SYNTHESIZER ARCHITECTURE

Instead we propose an alternative architecture based on injection locked frequency triplers (ILFTs) [4] and shown in Fig 2. The architecture first uses the original U-band (42-48 GHz) PLL with a 50 MHz reference and a single ILFD used to divide the carrier from 44 to 22 GHz to provide a low frequency input for the programmable CML divider. An injection locked buffer is inserted between the VCO and divider and used to drive the input of a D-band ILFT. Frequency alignment of the buffer is relatively easy as the frequency is identical to the VCO making the passives and devices used in both oscillators quite

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similar.

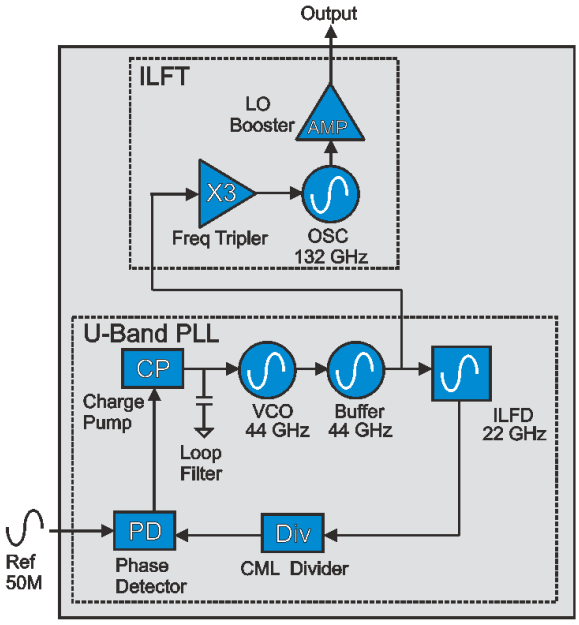

Fig. 2. Block diagram of the proposed D-band frequency synthesizer.

For the D-band application the U-band PLL will nominally run at 44 GHz near the center of it's lock range. The buffer drives an ILFT containing a non-linear amplifier which generates a large 3rd harmonic at 132 GHz used to injection lock an oscillator also running at 132 GHz. The ILFT restores signal swing and filters out the lower 44 GHz fundemental tone. Finally the ILFT output is provided by a small single-stage output amplifier used to boost the LO power for connection with a transmitter or receiver chain's mixer. While the proposed frequency synthesizer still contains many injection locked stages it removes one level of injection locking vs. the original cascaded ILFD architecture. Additionally since the high frequency D-band components are not directly inside the synthesizer's feedback loop the associated narrow locking range and limited output swing have little effect on the PLL's locking conditions. Since the original PLL can tune from 42-48 GHz, the generated third harmonic can sweep 3X this wide range (126-144 GHz), relaxing the frequency alignment at D-band. The synthesizer will lock provided the D-band oscillator's free-running frequency is within this range. The only critical alignment at D-band is the frequency of the output LO boosting amplifer must be well-aligned with the D-band oscillator's locking range to provide useful output power necessary to drive an output load (such as a mixer).

III. D-BAND ILFT DESIGN

Previously in [4] a common emitter stage usingh a SiGe HBT device was employed to provide the non-linearity required to generate odd harmonics. Unlike bipolar devices, CMOS common source stages exhibit very soft voltage waveform clipping, providing limited harmonic generation. For this reason the harmonic generation circuit shown in Fig 3 is used in the proposed D-band synthesizer. The employed tripler circuit contains complementary diode connected devices Q1 and Q3 to create waveform clipping at both the lower and upper half of the voltage swing and further increase generation of third order harmonic distortion components. Note that the 44 GHz buffer in the U-band PLL prevents device Q3 from loading the VCO and reducing voltage swing or creating startup problems.

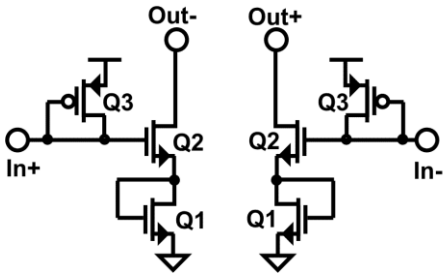

Fig. 3. Proposed harmonic tripler circuit with complementary diode connected devices Q1 and Q3 to improve harmonic generation.

The injection locking range of an oscillator can be described by $(I_{inj}/I_{osc})(f_o/2Q)$ where I_{inj} is the injected current, I_{osc} is the oscillator current, f_o is the center frequency and Q is the quality factor of the oscillator tank. To ensure locking in the proposed D-band synthesizer we control the oscillator current with a small current-steering 7 bit DAC as shown in Fig 4. This allows the I_{osc} current to be calibrated for maximium locking range while still ensuring correct start-up occurs. The oscillator tank is transformer coupled to provide output to the LO booster amplifier. A second DAC provides common-mode (CM) control of the LO booster output via the center-tap of an output transformer. While this function is not useful in the stand-alone chip, it allows a programmable bias to be applied to the LO port of a mixer of a connected transmitter or receiver chain. Both DAC's are controlled through the serial port of a desktop computer so all the settings can be calibrated during testing. Note the D-band oscillator contains no varactor or tuning capacitors as their inclusion would degrade voltage swing and possibly influcence oscillator startup. Also note the tuning range of the U-band PLL's 3rd harmonic (126-144 GHz) is much wider than the actual lock range of the ILFT (130.1-133.5 GHz).

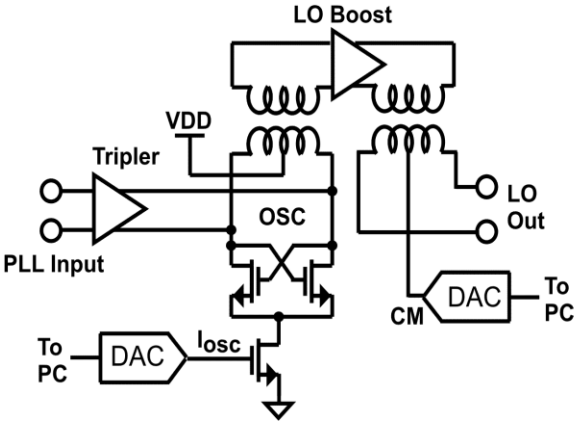

Fig. 4. D-band ILFT section of proposed synthesizer showing oscillator, control DAC for I_{osc}, LO booster and DAC for common mode adjustment.

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IV. MEASUREMENT RESULTS

Fig 5 shows the setup of the testing equipment used to characterize the proposed D-band frequency synthesizer. Also visible is the PC GUI used to control all of the digital settings for tuning of the PLL blocks and D-band ILFT section.

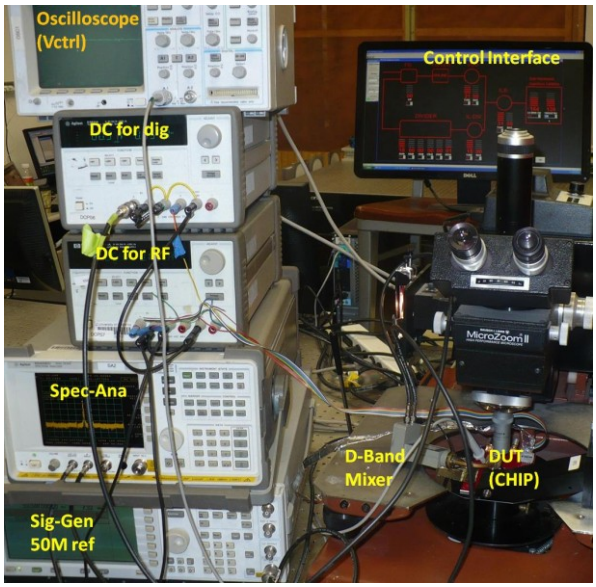

Fig. 5. Testing setup for characterizing the D-band frequency synthesizer showing instruments and digital control interface.

A D-band harmonic mixer in cascade with an Agilent 8565E spectrum analyzer was used in combination with a waveguide RF probe to perform measurements at the output of the LO Booster. The DC and control connections were wirebonded to a PCB. The on-chip LO booster (believed to be saturated) provides approximately -6 dBm of output power at 132 GHz as shown in Fig 6. The waveguide and probe losses were calibrated out of the measurements shown on the spectrum analyzer.

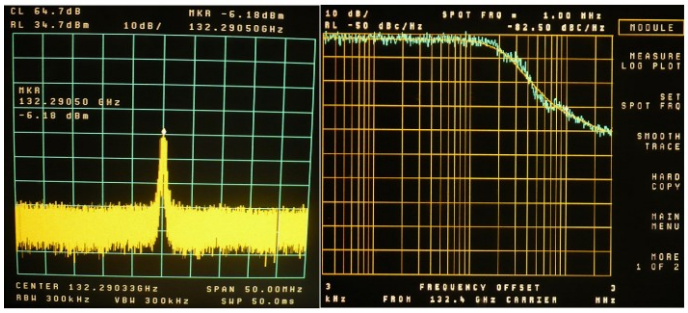

Fig. 6. Spectrum analyzer measurement showing 132 GHz tone from the output of the synthesizer and measured phase noise.

While the noise floor of the mixer and instrument is quite high, a phase noise measurement was still possible as shown in Fig 6. The measured spot phase noise was –82.50 dBc/Hz at 1 MHz offset from the 132 GHz carrier. The plot clearly shows that the in-band noise from the U-band PLL loop dominates and the D-band oscillator's phase noise is less critical. The lock range of the proposed frequency synthesizer was measured to be 130.15 GHz to 133.52 GHz which represents a tuning range of 2.5%

V. SUMMARY

The proposed D-band frequency synthesizer provides an alternative approach to cascaded ILFDs by employing sub-harmonic injection locking. The entire synthesizer uses 92mW of power and occupies 0.68mm^2 of silicon space while offering a phase noise of –82.50 dBc/ Hz at 1 MHz offset from 132 GHz. The performance is compared to other state of the art synthesizers in table 1. Finally Fig 7 shows a die photo taken of the proposed D-band frequency synthesizer with key blocks identified.

	[1]	[3]	[4]	This Work
Frequency	96 GHz	86 GHz	96 GHz	132 GHz
Phase Noise	-76 dBc/Hz @ 1 MHz	-83 dBc/Hz @ 1 MHz	-93 dBc/Hz @ 1 MHz	-83 dBc/Hz @ 1 MHz
Power	43.7 mW	65mW	140mW	92 mW
Area	0.7 mm^2	0.31 mm^2	1.8 mm^2	0.68 mm^2
Technology	65nm CMOS	65nm CMOS	180nm BiCMOS	65nm CMOS

Table 1. Comparison to state of the art mm-wave synthesizers.

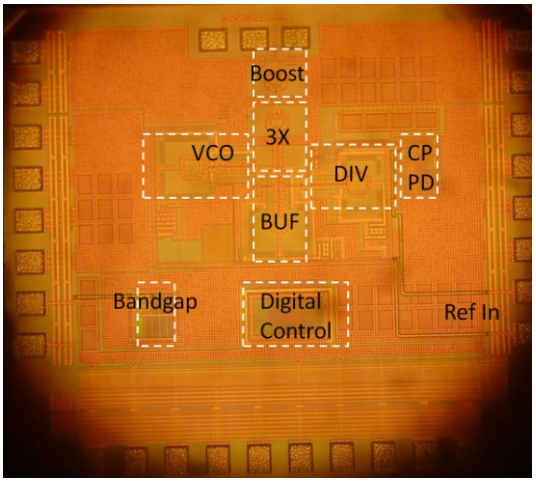

Fig.7. Die photo of the proposed D-band frequency synthesizer with major blocks identified.

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