

Embedded DiCAD Linear Phase Shifter for 57-65GHz Reconfigurable Direct Frequency Modulation in 90nm CMOS

Tim LaRocca, Jenny Liu, Frank Wang and Frank Chang

Department of Electrical Engineering, University of California, Los Angeles, CA, 90095, USA

Abstract — A digitally controlled artificial dielectric (DiCAD) differential transmission line is designed to perform agile linear phase shift over 100° with thermometer-coded 16step control. It also operates with a 16 gain-step VGA to enable re-configurable and direct-frequency modulation at 60GHz with 256^2 states (1.1° angular and 0.0007 magnitude resolutions) and -31dB static EVM for multiple PSK/QAM modulations. The modulator uses 0.33mm^2 core area in 90nm CMOS and consumes 10mA at 1V.

Index Terms — CMOS, Millimeter wave phase shifters, Permittivity, Quadrature amplitude modulation, Differential amplifiers.

I. INTRODUCTION

There is increasing demand for low-cost and high-performance millimeter-wave transmitters for digital communications while direct-frequency modulation is recognized as the most cost-effective solution for such transmitter design. Modern direct frequency modulator's performance is limited by its non-linear phase shifter. Passive phase shifters, for example, utilize bi-phase modulators which receive reflected signals from a variable resistance cold-FET [1] or varactor [2] via a 90° hybrid. Resistance/capacitance variation may change their phase and precise bias controls are necessary to track the nonlinear R-V or C-V relationship. Active phase shifters on the other hand utilize variable-gain amplifiers and multiple passive hybrids/combiners to create the phase shift [3]. In such cases, modulator performance is adversely sensitive to the phase/gain mismatch between amplifiers, differential hybrids and nonlinear phase controls.

In this paper, we use embedded DiCAD (digital controlled artificial dielectric) differential transmission lines (DTL) (detailed in Section II) in 90nm CMOS to circumvent non-linear phase shift issues and realize a reconfigurable direct-frequency modulator for 57-65GHz applications. Key design challenges include:

- 1) Create embedded DiCAD-DTL in CMOS interconnect metals;
- 2) Insert high speed and low loss NMOS π -switch to control DiCAD permittivity;

- 3) Generate linear phase shift in DiCAD-DTL with 4:16 bit thermometer encoder;

- 4) Design quadrant phase and amplitude shifters (QPAS) with DiCAD-DTL for both phase shift and amplifier impedance matching;

- 5) Finalize a compact and re-configurable direct-frequency modulator without traditional DAC, mixers, filters, LO hybrids, varactors and reflective devices in Fig.1.

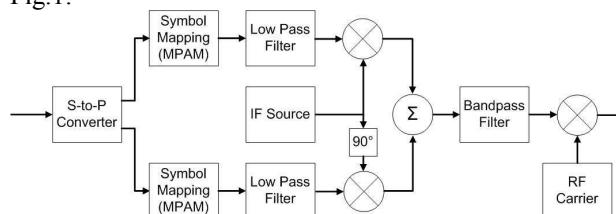


Fig. 1. Generic QAM transmitter including DAC (symbol mapping), IQ modulator, upconverter and filtering.

A re-configurable millimeter-wave direct frequency modulator would be attractive to both commercial and military markets. This flexible design supports the newly released 60GHz standards WirelessHD, IEEE WPAN 802.15.3c and ECMA TC48 which define multiple classes of operation for different applications depending on distance and functionality. Each class specifies a certain data rate from roughly 50Mb/s to beyond 3Gb/s with different modulation schemes and coding. The modulation schemes vary from $\pi/2$ -BPSK, $\pi/2$ -QPSK, $\pi/2$ -Star 8QAM, $\pi/2$ -16QAM, and OOK. Fig.2 illustrates three of these schemes. In order to comply with the entire standard, the transmitter and receiver must be adaptable or reconfigurable to handle various modulation schemes.

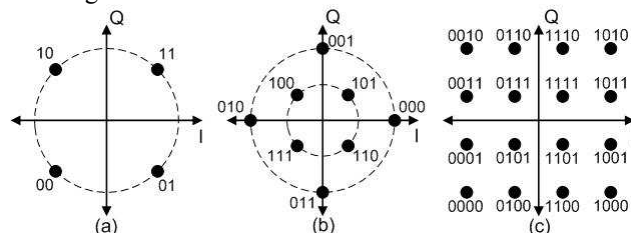


Fig. 2. (a) $\pi/2$ -QPSK, (b) $\pi/2$ -Star 8QAM, and (c) $\pi/2$ -16QAM modulation schemes for 60GHz.

II. DiCAD

DiCAD was introduced by authors in [4] to digitally control the permittivity, $\epsilon_{r,\text{eff}}$, of a DTL. It is comprised of UMC 1P9M digital CMOS metal layers (Fig.3), where M8 and M9 are combined to form a 2.25 μm thick DTL and M7 and M6 to form the underlying floating strips. NMOS π -switches are inserted along the DTL virtual ground line, bisecting strips, and turning “on” or “off” individual strip to engage/disengage it from the DiCAD in order to vary its $\epsilon_{r,\text{eff}}$ roughly from 18.8 (all switches off) to 32.5 (all switches on), Fig. 4.

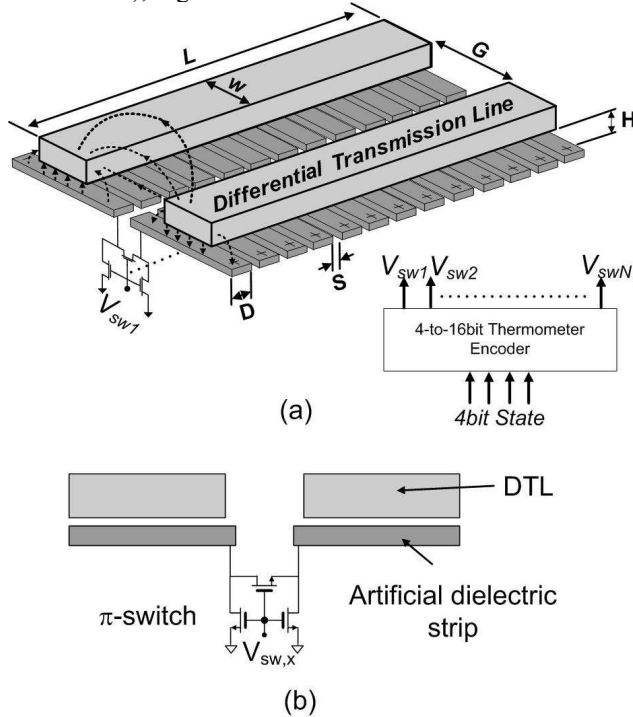


Fig. 3. (a) General DiCAD differential transmission line layout, (b) cross-sectional view of DiCAD DTL strip.

The backbone of the modulator is a 48.5 μm (L) DiCAD element with 15 strips 3 μm in width (D) and 0.5 μm spacing (S) in an open-circuited (O.C.) stub configuration, which maximizes the artificial dielectric effect while maintaining a compact size. The DTL width (W) is 20 μm and spacing (G) is 10 μm . An on-chip 4bit thermometer encoder offers 16 individual digitally controlled ON/OFF states. State 0000 turns off all strips, state 0001 turns the first strip on, state 0010 turns the first 2 on until state 1111 turns all strips on. A test structure with these dimensions and encoder was measured at 62GHz. An Agilent E8371A network analyzer and custom SOLT calibration standards were used. This open stub DiCAD transmission line effectively varies the phase of S11, in Fig. 4, from -46.1 $^\circ$ to -72.3 $^\circ$, which is sufficient for implementing the desired vector modulator.

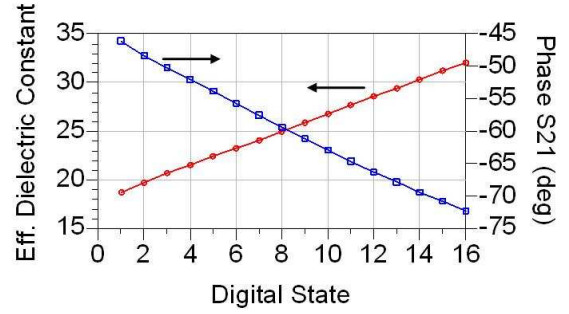


Fig. 4. Measured effective dielectric constant and S21 phase shift (deg) at 62GHz of a 48.5 μm open-circuited DiCAD stub across 16 digital states.

The switch network consists of three NMOS devices in a π -configuration (Fig.3b). Two shunt NMOS devices are used to create DC paths for the center NMOS switch, while keeping the DiCAD strips floating to eliminate the effect of gate leakage on the center switch’s gate-to-source voltage. There is a tradeoff between parasitic “on” resistance and “off” capacitance of the center switch for insertion loss and isolation, respectively. As a result, the center switch gate length is chosen as the regular 90nm with total gate periphery of 3.52 μm divided into 4 fingers. π -switches are estimated with the worst “off” and “on” settling times of 40ps and 20ps, respectively, as switched directly between 0000 to 1111 states as shown in Fig.5.

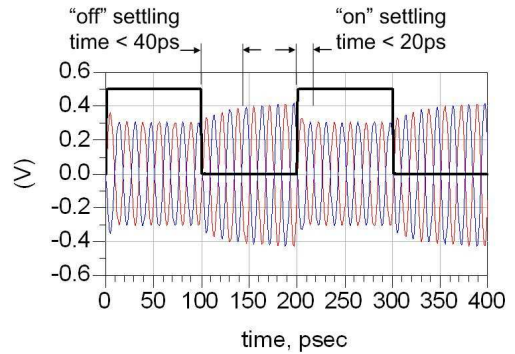


Fig. 5. DiCAD DTL’s settling times estimated to be $<40\text{ps}$.

III. DESIGN

The direct-frequency modulator (Fig.6) operates by summing two vectors of \vec{A} (QPAS 1) and \vec{B} (QPAS 2) [3]. If \vec{A} covers all of quadrant I ($0 < |r_A| < \infty$ and $0 < \theta_A < \pi/2$), and \vec{B} covers the diagonally opposite quadrant III ($0 < |r_B| < \infty$ and $-\pi/2 < \theta_B < \pi$), the resultant vector \vec{R} then covers the entire coordinate system.

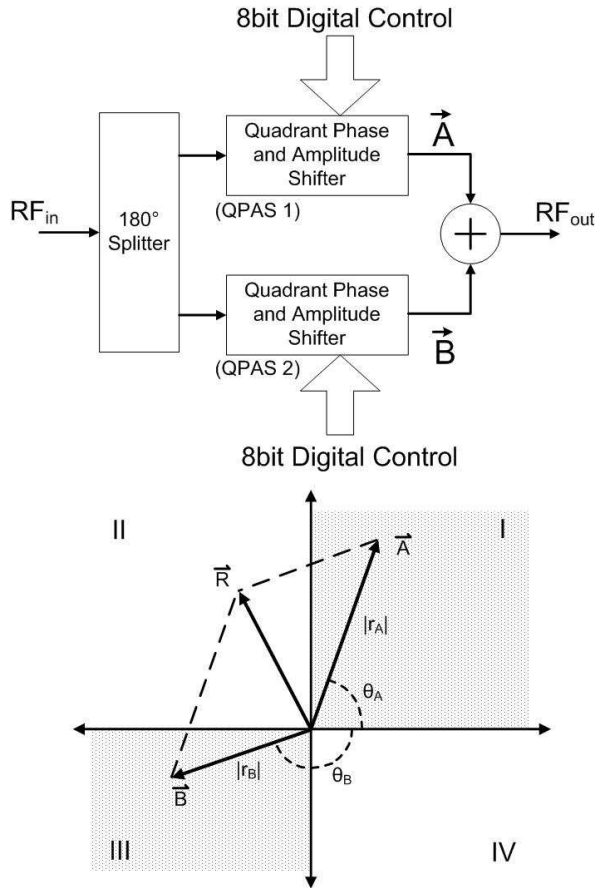


Fig. 6. Block diagram and vector plot of direct frequency modulator.

The quadrant phase/amplitude shifter (QPAS) is implemented with both O.C. (open-circuited) and S.C. (short-circuited) stub DiCAD-DTLs. The schematic is shown in Fig. 7. Phase and amplitude control are each 4bits. The digital amplitude control is based on an off-chip DAC. Each QPAS is designed as a conjugately matched amplifier with the DiCAD elements folded into the input and output matching networks. These networks are dynamic element matching (DEM) networks which vary the phase similar to a Lo-Hi-Lo low-pass phase shifter, which is a shunt-C:series-L:shunt-C network. In this case, the shunt-C is replaced with a variable O.C. DiCAD DTL stub which can be digitally controlled to obtain a linear phase response.

The NMOS common source, CS, differential pair ($L=90\text{nm}$ $W=2\mu\text{m}$ with 8 fingers) is matched to 50Ω using the described O.C. DiCAD stubs and series inductors for input and output networks. Bias is tapped at the virtual ground of S.C. DiCAD stubs. Amplitude or gain is controlled by varying gate voltages of the NMOS differential pair and thus changing their I_{DS} and g_m .

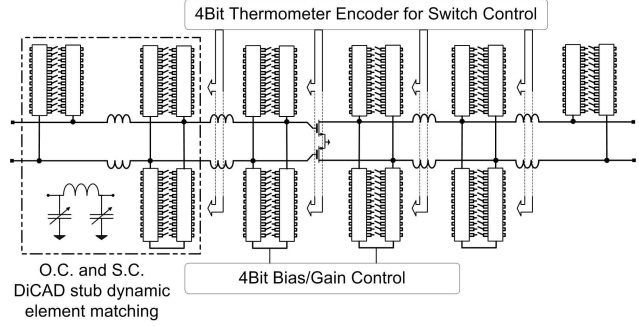


Fig. 7. QPAS schematic including O.C. and S.C. DiCAD stub dynamic element matching and differential CS amplifier.

IV. RF PERFORMANCE

Measurements validate the QPAS design for 62.64GHz , one of the 4 required $802.15.3c$ carrier frequencies, as plotted in Fig. 8. The QPAS covers an entire quadrant, as described in the previous section, controlling the phase and amplitude of vector A or B. The modulator has 16 different phase states and the NMOS gate voltage, V_g , is varied between 0.3V to 0.675V in 25mV steps (4bit). This results in a total of 256 vector points per QPAS.

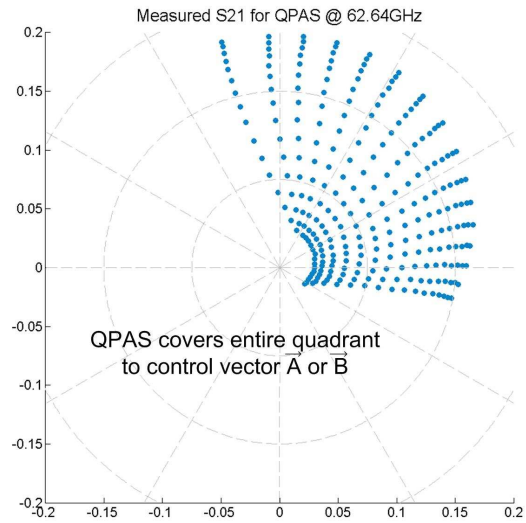


Fig. 8. Measured QPAS performance at 62.64GHz for all 256 states (16 phase states \cdot 16 amplitude states). Similar results for 58.32 , 60.48 and 64.8GHz $802.15.3c$ channels.

All 256^2 combinations were swept in our test of the reconfigurable modulator and the results are shown in Fig. 9. The test equipment was GPIB controlled using LabVIEW and included a NI 6008 DAQ for digital control, power supplies and E8371A Agilent network analyzer. Average resolution between states is 1.1deg and $7e-4$ in magnitude.

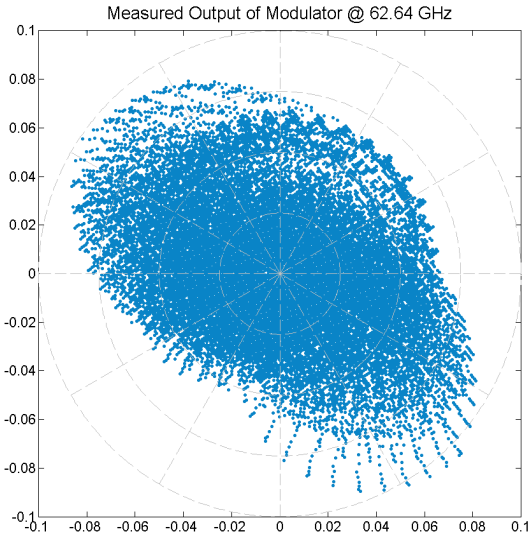


Fig. 9. Measured modulation states (256^2) at 62.64GHz.

The states can be pre-programmed and selected for the corresponding modulation schemes as shown in Fig.10. The measured static EVM for each state is -31dB without any compensation. Programming details for the QPSK schematic are shown in Table I.

Table I. QPSK Constellation Input Information

QPSK State	QPAS 1 Inputs		QPAS 2 Inputs	
	Phase (4b)	Vg (4b,V)	Phase	Vg
00	1111	0101, 0.425	0010	1101, 0.625
01	1000	1011, 0.575	0000	0011, 0.375
11	0101	1011, 0.575	1111	0101, 0.425
10	0000	1010, 0.55	0110	1111, 0.675

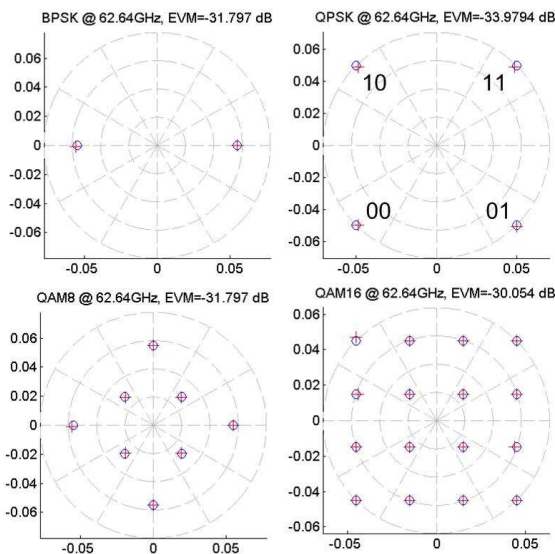


Fig. 10. Measured modulation states (+) and ideal states (o).

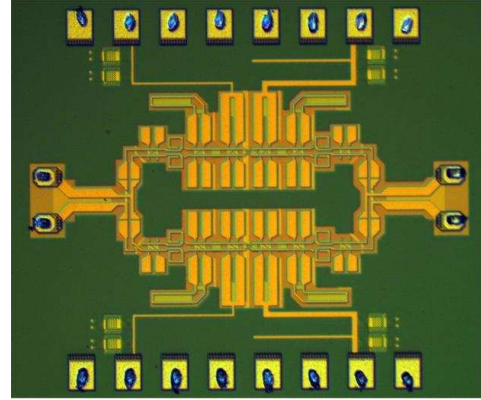


Fig. 11. Modulator die photo. Core area of 0.65mm x 0.5mm.

V. CONCLUSION

We have devised a DiCAD based linear phase shifter which is embedded in standard 90nm CMOS process with NMOS π -switches for digital phase control. We also use a differential amplifier for amplitude control to realize the intended 57-65GHz reconfigurable direct-frequency modulator covering multiple m PSK/QAM modulations. The measured static EVM for each modulated state at 60GHz is better than -31dB without any compensation and if necessary, we can also compensate EVM errors due to process variations by using the 256^2 available states with sufficiently fine resolutions. The resultant modulator contains 10 DiCAD-DTL, 276 π -CMOS switches, 1 NMOS differential amplifier and consumes average 10mW under 1V power supply. This modulator can be integrated with our recently demonstrated high PAE CMOS power amplifier [5] to form a reconfigurable transmitter for 57-65GHz communication systems.

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