A Fractional-*N* PLL for Multiband (0.8–6 GHz) Communications Using Binary-Weighted D/A Differentiator and Offset-Frequency Δ-Σ Modulator

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***Abstract*—A compact, low power and global-mismatch-tolerant 0.8–6 GHz fractional-*N* PLL is designed to cover IEEE 802.11abg, PCS/DCS and cellular bands. Two new techniques are proposed to cancel the in-band quantization noise and fractional spurs. Firstly, a second order binary-weighted digital/analog differentiator (DAD) is utilized to enable the second order mismatch shaping and reduce the quantization noise by 25 dB, along with advantages of compact circuit implementation with smaller routing area and less power consumption over those of dynamic element matching (DEM) based counterparts. Secondly, mechanisms causing fractional spurs are also identified and a third order offset-frequency delta-sigma (Δ-Σ) modulator is devised to decrease the in-band spurs by 20 dB in simulation and 8 dB in present single-ended circuit implementation.**

***Index Terms*—Fractional-*N*, phase-locked loop (PLL), multiband frequency synthesizer, delta-sigma modulation, digital-analog conversion, binary-weighted digital-analog differentiator (DAD), mismatch shaping, quantization noise, fractional spurs, offset-frequency delta-sigma (Δ-Σ) modulator.**

I. Introduction

As THE wireless industry continues to evolve, many portable devices are designed to fulfill ever-increasing standards at various frequency bands. For example, Bluetooth and WLAN are being integrated into multiband cellular phones. As a result, a frequency synthesizer with wide tuning range, fine frequency resolution, good phase noise and low power consumption becomes an essential building block for such system designs. In principle, wide tuning range can be achieved by multiplying, dividing or mixing the output frequency of a phase locked loop (PLL) for the intended band coverage. Among all types of PLLs, the fractional-N PLL is most favored due to its flexibility and fine resolution in frequency tuning. The PLL-divided frequency can be locked to a relatively high reference frequency, unbounded to the minimum channel spacing within all desirable standards. The high reference frequency also permits a wider-loop bandwidth for reducing in-band VCO phase noise. However, PLL's division residue often creates extra phase noise near the frequency of operation and can only be resolved with a delta-sigma (Δ-Σ) modulator to convert the quantization noise to higher frequencies and eliminate it with a narrow bandwidth loop filter. The choice of the loop filter bandwidth must thus trade off filtering between the quantization noise and the in-band VCO phase noise. Such trade-off can be relaxed sometimes by feeding amplitude-modulated pulses via DAC to compensate pulse-width-modulated charge pump currents caused by the quantization noise. Consequently, wider loop bandwidth may be maintained. Such designs nonetheless inevitably encounter the following design issues:

First, effective quantization noise cancellation depends strictly on high charge pump linearity and low DAC mismatch. Techniques were proposed in the past to shape the DAC mismatch [1]–[4], but all with constraints. For instance, the dynamic element matching (DEM) method demands extensive digital signal processing (DSP) to surmount mismatch effect due to process variation and often renders mismatch shaping to first order. The widely used thermometer-coded [1]–[3] or fully-segmented DAC [4] consumes either large routing area or twice the number of DAC units. Second, reduced fractional spurs can only be achieved by increasing the charge pump linearity. A non-delta-sigma quantizer was proposed to suppress fractional spurs [5]. The added noise, however, could not be rejected by high-pass function and therefore degraded PLL's in-band SNR.

In this paper, two techniques are applied to mitigate aforementioned PLL design issues [6]. A second order binary-weighted D/A differentiator (DAD) is used to obtain second order mismatch shaping, without DEM and thermometer-coded DAC. In addition, a third order offset-frequency Δ-Σ modulator is used to alter the fractional frequency and prevent fractional spurs from falling in the loop bandwidth. Fig. 1 shows the block diagram of the proposed fractional-N PLL. With VCO operating from 3.2 to 4 GHz, multiple 802.11abg, PCS/DCS and cellular bands can be covered via a direct conversion architecture. With 20 MHz reference frequency and a 21-bit third order Δ-Σ modulator (MASH-111), frequency resolution can be as fine as $20/2^{21}$ MHz.

The underlying circuit design techniques are detailed in subsequent sections. Section II describes the architecture of second order binary-weighted DAD and its unique advantages. Section III discusses the algorithm of offset-frequency Δ-Σ modulation for eliminating sources of spurs. Section IV describes actual circuit implementation of overall PLL and

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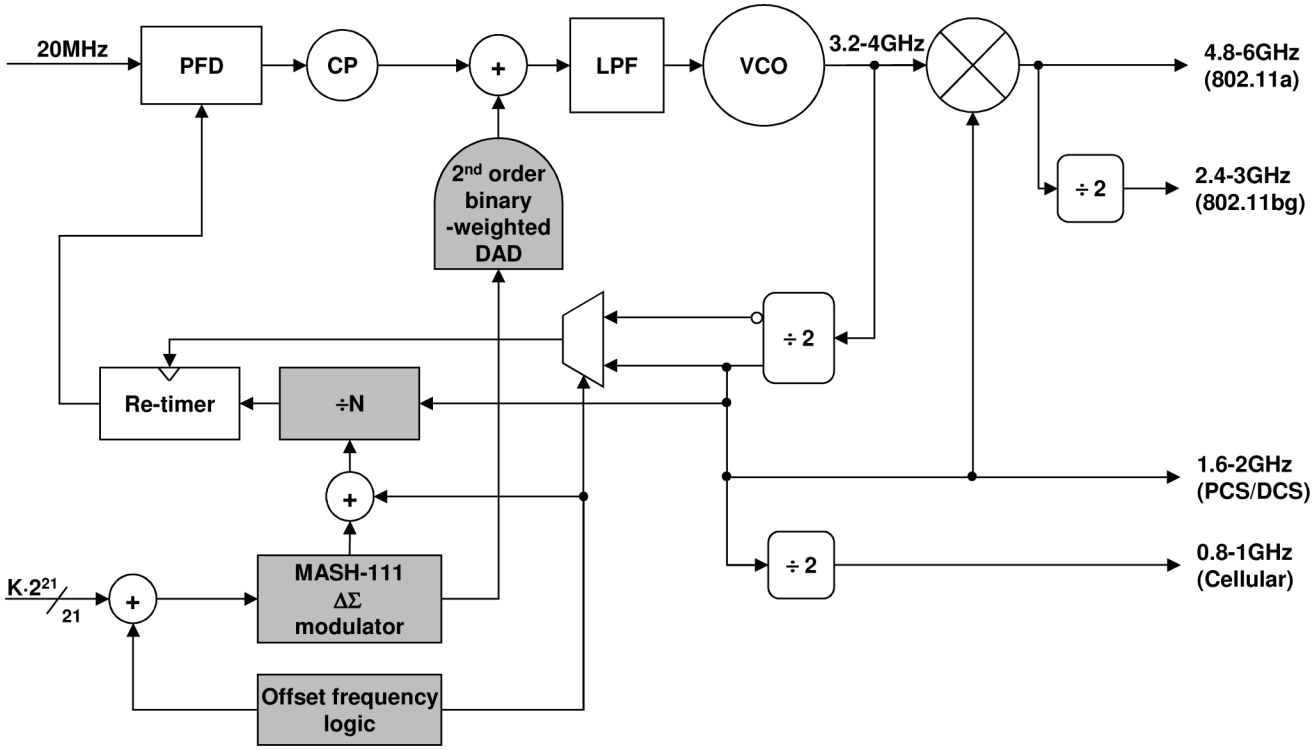


Fig. 1. Block diagram of 0.8–6 GHz fractional-N PLL.

Section V shows its test results. Finally, we conclude the paper in Section VI.

II. Quantization Noise Cancellation

A. Issues on Quantization Noise Cancellation

The characteristic of quantization noise appears to be random in nature but in fact is deterministic. It can be obtained by integrating the difference of the Δ-Σ odulator I/O [7] and cancelled by summing its inversed signal through a DAC at the charge pump output. However, two potential issues may limit such a cancellation scheme. First, since high bit-width Δ-Σ odulator is required to achieve fine frequency resolution, a second quantizer must be used to truncate the cancellation signal for utilizing rational DAC complexity. Under such circumstances, additional quantization noise will be introduced to PLL by the second quantizer. To avoid it, additional Δ-Σ modulator is needed to shape the noise, but would take excessive hardware for implementation [1]–[4].

Second, mismatch among individual DAC elements creates extra phase noise. DEM has been popularly used to convert element mismatch to white noise [1] or first order high-pass color noise [2], [3] in the thermometer-coded DAC architecture. Large routing area and high DSP power are the drawbacks. It can also be implemented with the fully-segmented DAC architecture [4], but costs twice the number of DAC units [8]. The block diagram of the prior implementation is shown in Fig. 2.

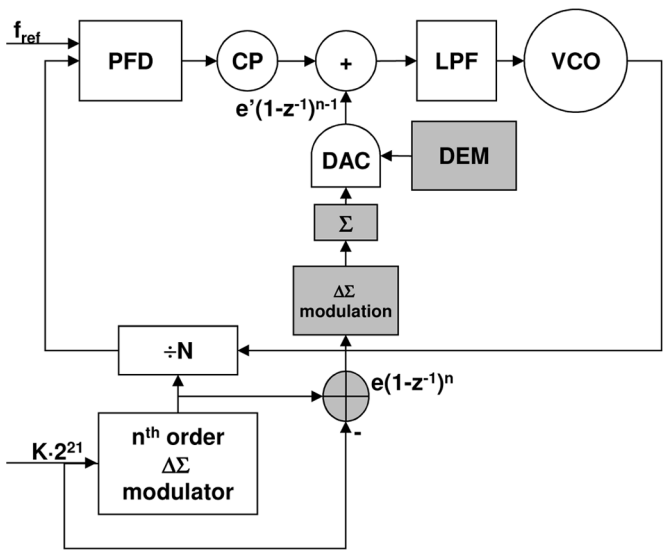


Fig. 2. Conventional mismatch shaping DAC.

B. MASH-111 With Differentiators

In this work, MASH-111 is used to implement third order Δ-Σ odulator. Aside from its unconditional stability and low complexity, MASH-111 also has the advantage of tapping out the unprocessed quantization error, e, directly in Fig. 3. It is much simpler to generate a cancellation signal from the unprocessed quantization error. The second 6-bit quantizer, which is needed to limit the DAC bit-width, can be directly added. Three subsequent differentiators are supposedly needed to obtain the noise cancellation signal, $e(1-z^{-1})^3$ and high-pass filter the second quantization noise, e_2. But none of them are required in this implementation, because one can be functionally neutralized by a subsequent integrator, which imitates the frequency to phase conversion in the cancellation path, and the other two can be merged with four DAC elements to form a second order

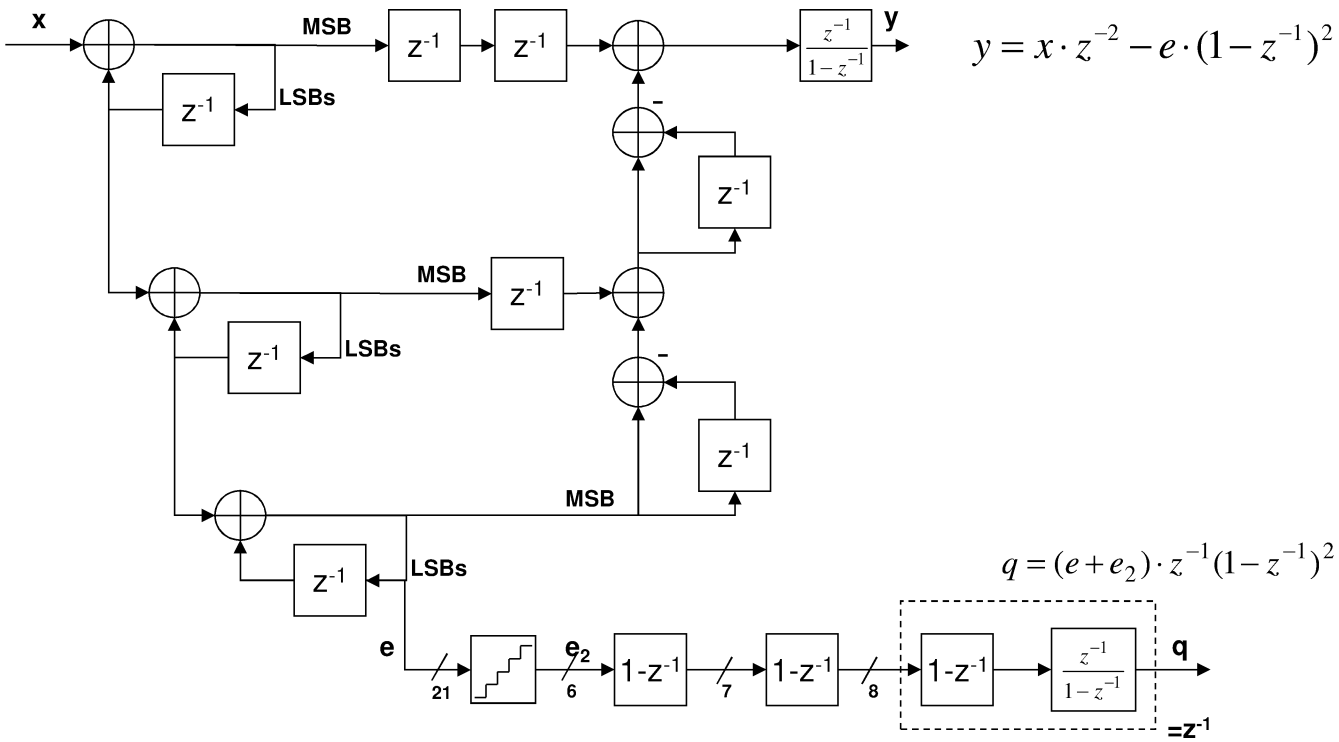


Fig. 3. Cancellation signal generated by MASH-111 Δ-Σ modulator with differentiators.

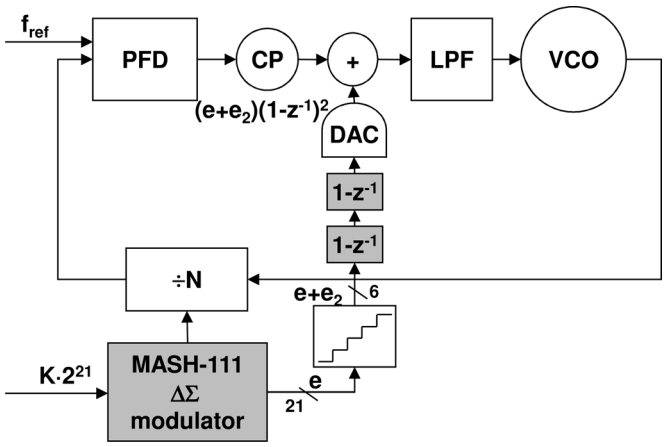


Fig. 4. Fractional-N PLL with MASH-111 Δ-Σ modulator and differentiators.

DAD. This unique arrangement in Fig. 4 saves an adder, integrator and the second Δ-Σ modulator as compared with the implementation in Fig. 2.

C. Second Order Binary Weighted D/A Differentiator

The binary weighted D/A differentiator was originally proposed for delta-sigma D/A converters [9]. It is also suitable for cancelling the quantization noise in the fractional-N PLL. The second order binary-weighted DAD renders the second order high-pass shaping function to multi-bit DAC mismatch and requires no additional DSP. Second order DAD can be configured by embedding four DAC elements into two-stage cascaded differentiators to realize the $(1 - z^{-1})^2$ function, as shown in Fig. 5. The mismatch from each DAC element is assumed to be a, b, a_2, and b_2, respectively. As the signal swaps every other clock cycle at the first stage output, $p_1\ (n)$ and $p_2\ (n)$ will form complementary pairs. Subsequently, the only possible values at outputs of second stage differentiators, $[p_1(n), -p_1(n+1)]$ and $[p_2(n), -p_2(n+1)]$, are either [(0, 1), (1, 0)] or [(1, 0), (0, 1)]. Therefore, the errors at output of the left DAC pair can only be [(0, a), (b, 0)] or [(a, 0), (0, b)]. Taking discrete Fourier transform of these sequences, the summed output noise at the left half of the second order DAD becomes

$$\boldsymbol{E}_a(z) + \boldsymbol{E}_b(z) = \frac{\pm(\boldsymbol{a} - \boldsymbol{b}z^{-1})}{2}(1 - z^{-1}). \tag{1}$$

If the mismatch between two DAC elements is identical, $a = b$, a second order shaping function can be achieved:

$$\boldsymbol{E}_a(z) + \boldsymbol{E}_b(z) = \frac{\pm\boldsymbol{a}}{2}(1 - z^{-1})^2. \tag{2}$$

If two elements are unmatched, we can rewrite a and b in terms of the common mode mismatch, u, and the differential mode mismatch, v, and substitute them in (1):

$$\boldsymbol{E}_a(z) + \boldsymbol{E}_b(z) = \frac{\pm\boldsymbol{u}}{2}(1 - z^{-1})^2 + \frac{\pm\boldsymbol{v}(1 + z^{-1})}{2}(1 - z^{-1}). \tag{3}$$

Similar expressions can be derived for the right half of the second order DAD. According to (3), as long as the differential mismatch between adjacent elements is minimized, second order mismatch shaping can be realized. Consequently, the stringent requirement on the global matching of a traditional multi-bit DAC can be relaxed to the local matching between adjacent DAC elements. This can be easily accomplished by

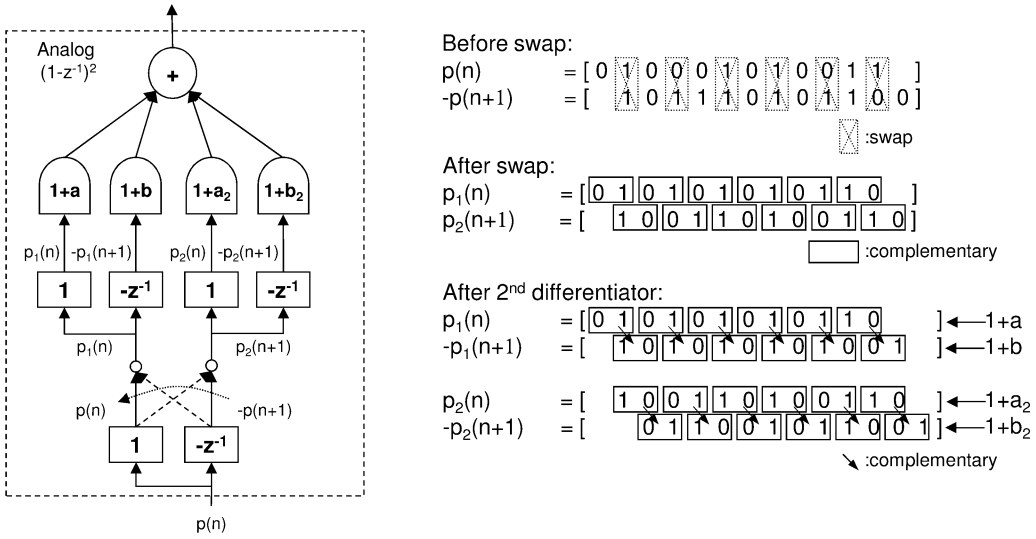


Fig. 5. Second order mismatch shaping using second order DAD.

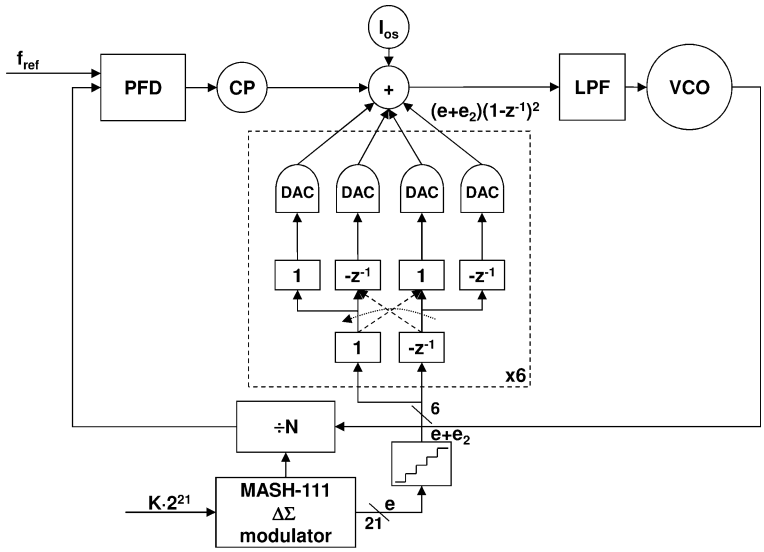


Fig. 6. Second order binary-weighted DAD implantation in fractional-N PLL.

routing symmetric adjacent cells with inter-digitated structure to minimize the process mismatch.

The multi-bit DAD can also be implemented with binary-weighted architecture without suffering from large differential non-linearity (DNL) in Fig. 6. It is because gain error in each binary-weighted DAD element can be treated as the common-mode mismatch and filtered by second order high-pass function. There are three advantages of second order binary-weighted DAD over first order thermometer-coded or fully-segmented DAC with DEM. First, the second order or common mode mismatch shaping can tolerate bigger mismatch due to process variation and routing parasitics. In fact, it offers 20 dB more reduction in simulation with the same mismatch condition [9]. Second, the DAD implementation does not require DSP power compared to DEM implementations. Finally, the binary weighted DAD uses less DAC elements than a thermometer-coded DAC and it occupies half the area of a fully-segmented DAC.

III. Fractional Spurs Reduction

A. Origins of Fractional Spurs

Fractional spurs were generally referred to phase noise induced by fractional-N PLL's quantization error [1], [10]. In this work, we defined fractional spurs specifically as high power density tones appearing near the carrier frequency. Although quantization noise can also create high power density tones in the frequency spectrum, they can be removed simply by dithering [18]. Fractional spurs caused by circuit distortions, however, cannot be eliminated by using dithering and are particularly undesirable for communication systems.

Two major types of circuit distortion would cause fractional spurs. The first is the coupling between the reference frequency and the output frequency. For instance, Nth harmonic of the reference frequency can be forward-coupled to VCO output via the PFD and charge pump through parasitics [5]. Another example

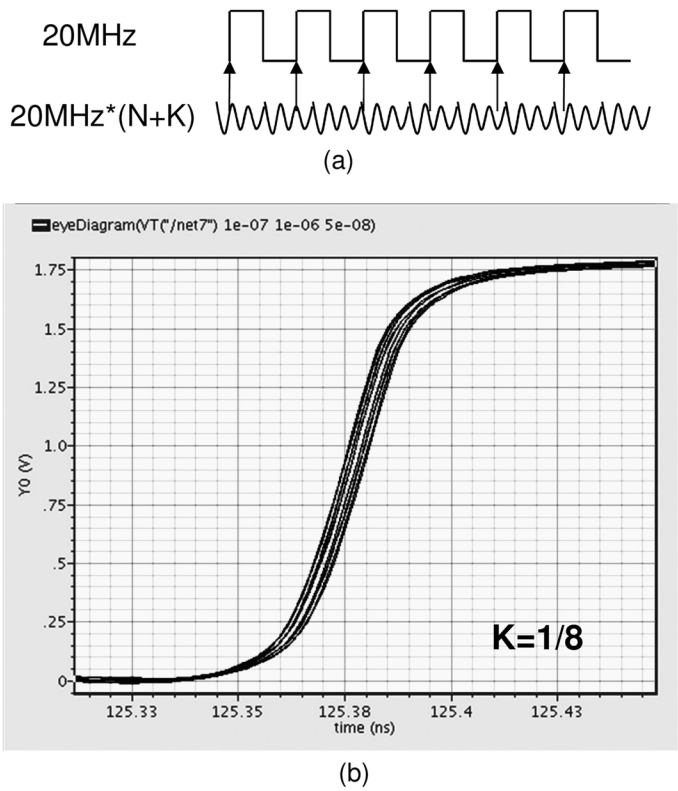


Fig. 7. (a) Reference clock edge modulated by modulus divider input. (b) Induced clock jitter.

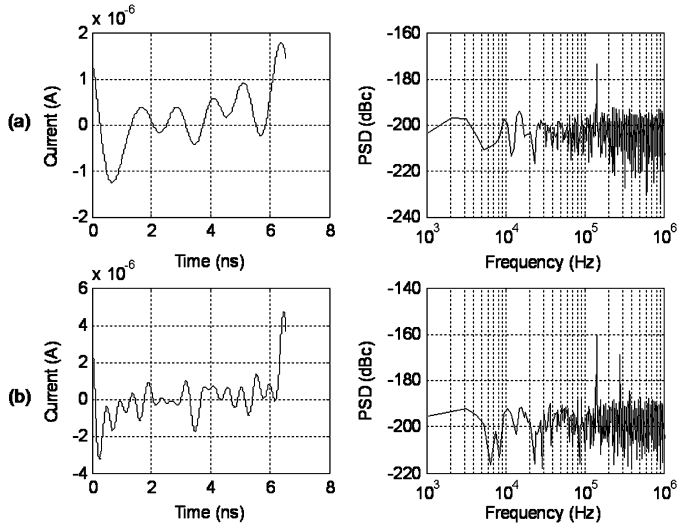


Fig. 8. (a) Fractional spurs under slow varying charge pump current non-linearity; (b) under fast varying charge pump current non-linearity.

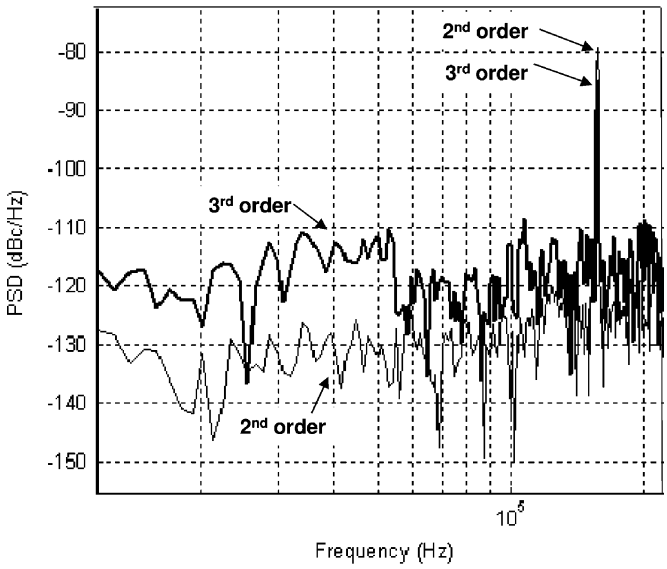


Fig. 9. Fractional spurs comparison between second and third order Δ-Σ modulators.

is that the input frequency of the modulus divider can be reverse-coupled to the crystal oscillator or buffer through the conductive substrate to alter the reference clock edge. This effect is illustrated in Fig. 7. When the divisor is $N + 1/8$, the reference frequency is split into 8 rising edges with different delays, causing fractional spurs to be generated at 20 MHz/8. Fortunately, such fractional spurs are independent of the Δ-Σ modulator operation and typically less powerful than their Δ-Σ modulator dependent counterparts (the second type) as explained below.

As a non-linear feedback system, the Δ-Σ modulator with fractional K input should have a limit cycle of $1/K$ [18]. Consequently, its quantization error sequence can be split into an accumulative sequence of K and a random sequence of integers, n. The limit cycle will also appear as the rising edge timing variation in PLL's charge-pump against the reference clock. Again, the timing variation would have an accumulative time sequence of $K \cdot T_{\rm div}$ plus a random time sequence of $n \cdot T_{\rm div}$, where $T_{\rm div}$ represents the input period of the modulus divider. Under the influence of circuit non-linearity, such time sequences would generate fractional spurs in the frequency spectrum. For instance, we can decompose the non-linearity generated during the rising edge time window of the charge pump into various frequency components. When the frequency coincides with $1/T_{\rm div}$, the specific non-linearity will be sampled at every $K \cdot T_{\rm div}$ with sampled value reproduced at the limit-cycle rate, or at the fractional frequency, $f_{\rm fract}$, which equals the reference frequency $(f_{\rm ref})$ multiplied by K. Nonetheless, the random time sequence of $n \cdot T_{\rm div}$ on the rising edge has no effect on sampling because the non-linearity repeats itself every $T_{\rm div}$. When the frequency of the non-linearity occurs at multiples of $1/T_{\rm div}$, higher harmonics of fractional spurs appear. As shown in Fig. 8, when the non-linearity varies in higher rate, the second harmonic tone starts to emerge. In Fig. 9, the lower noise floor explains the second order Δ-Σ modulator is actually less sensitive to the non-linearity, since the window of the rising edge time is narrower. However, the higher spurs level indicates the non-linearity with frequency of $1/T_{\rm div}$ is more likely to prevail within the narrower window for the second order Δ-Σ modulator than its third order counterpart.

Therefore, one may eliminate fractional spurs by reducing either circuit non-linearity or Δ-Σ modulator limit cycle. Several

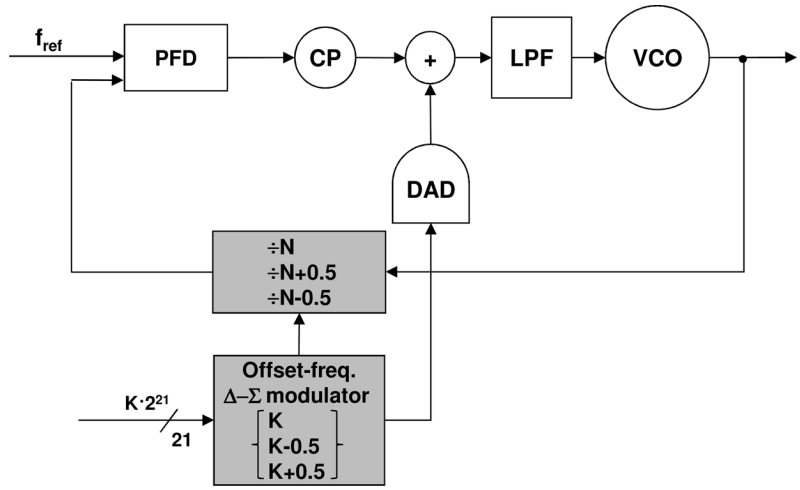


Fig. 10. Fractional-N PLL with offset-frequency Δ-Σ modulator.

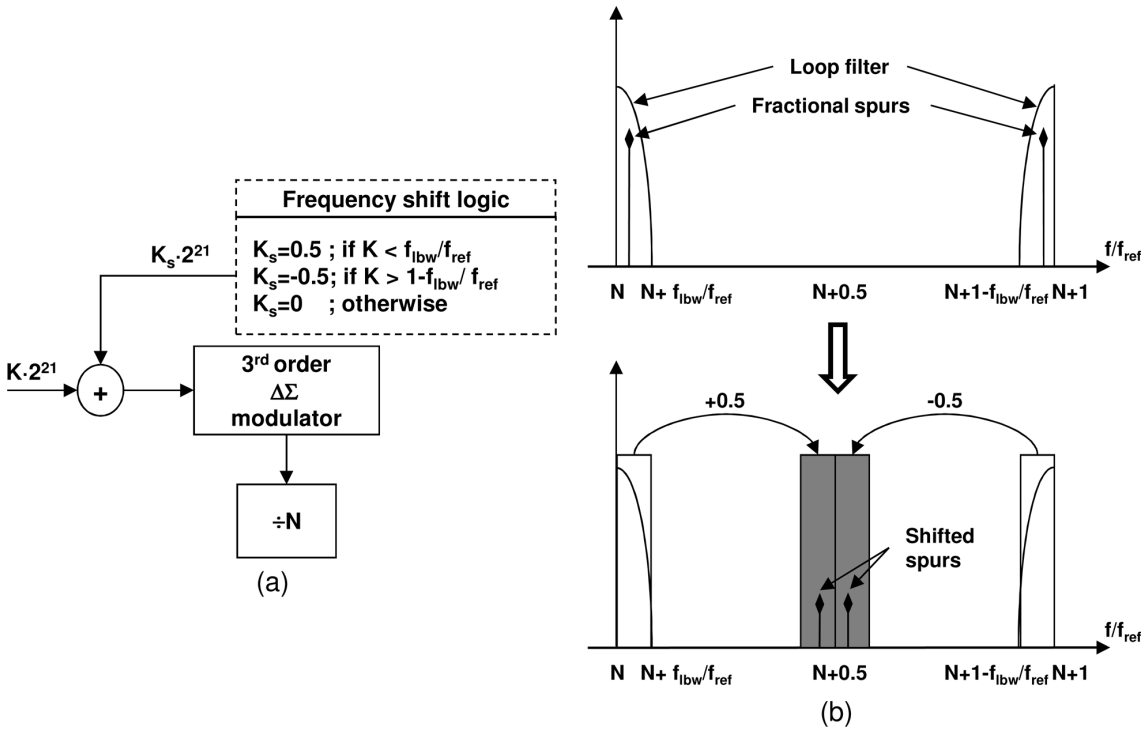


Fig. 11. (a) Frequency shift algorithm. (b) Frequency shift for minimizing fractional spurs.

techniques were proposed in the past to eliminate circuit distortions. For example, current mismatches in the charge pump can be reduced by adding offset current [3], [11]. Modulus dependent divider delay can be decreased by re-sampling [17] and DAC mismatch can be solved by DEM or DAD.

To avoid issues of limit cycle, [5] proposed to eliminate Δ-Σ modulator but at the expense of its benefit of simplicity. In principle, one may also shift the fractional frequency to reduce in-band fractional spurs, since fractional spurs falling beyond the loop filter bandwidth will be considerably rejected. Intuitively, one may vary the reference frequency to allocate the fractional frequency distant from the loop filter bandwidth. However, the reference frequency is provided by a crystal oscillator and any attempt to alter the timing of a crystal oscillator would corrupt its frequency precision and phase noise. The correct alternative would be to modify the fractional divisor, K. For example, giving $N + K$ as $99.5 + 0.51$ to relocate the fractional frequency, the consequent fractional spurs will appear at 10.2 MHz from the carrier and can be easily eliminated by using a loop filter. We developed this unique frequency-offset method to suppress fractional spurs with details disclosed as follows.

B. Offset-Frequency Δ-Σ Modulator

By re-partition the divisor between the Δ-Σ modulator (K) and the frequency divider (N), the fractional spurs can be

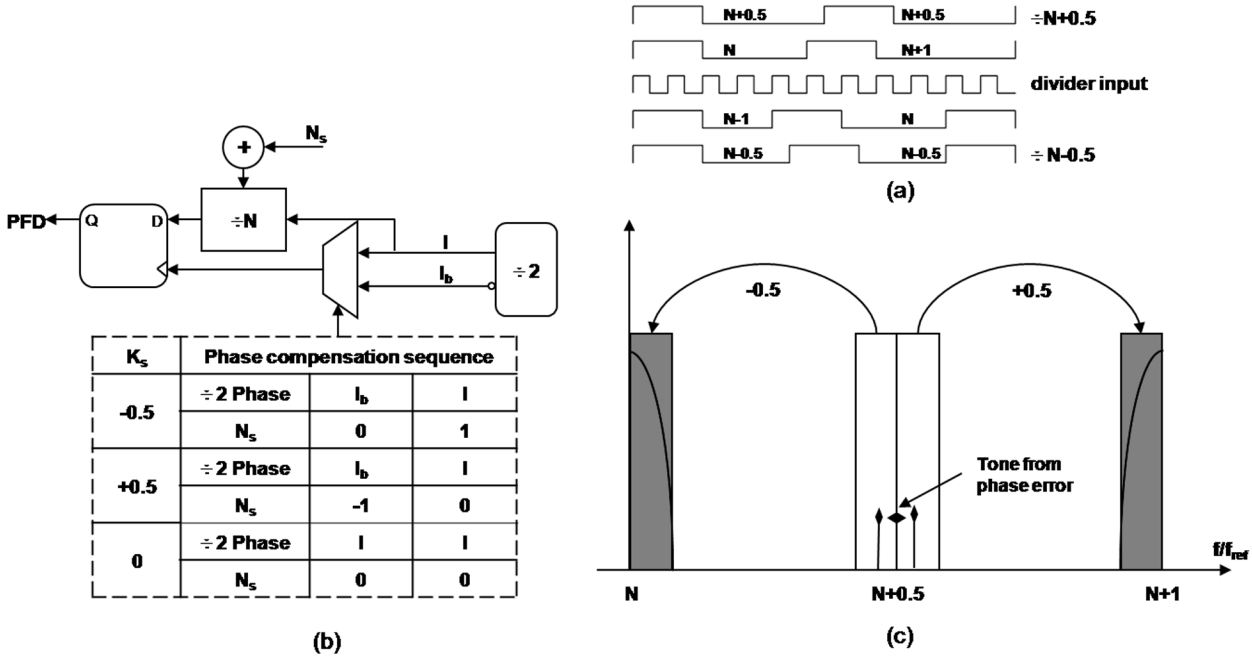


Fig. 12. (a) Half modulus divider timing diagram; (b) Phase compensation sequence; (c) Phase compensation to shift the carrier frequency.

suppressed. Fractional frequency dividers must be employed in order to shift the divisor in fractions. It may be chosen to shift the divisor by 0.5 as for its easiness in implementation and effectiveness in moving fractional frequency far away in frequency spectrum. For instance, the frequency divider will divide the input frequency by fractional numbers of 98.5, 99.5, 100.5, and 101.5 rather than integer numbers of 98, 99, 100, and 101. Consequently, the offset-frequency Δ-Σ modulator needs to shift either $+0.5$ or -0.5 to maintain the same divisor. Fig. 10 shows the block diagram of the proposed fractional-N PLL with the offset-frequency Δ-Σ modulator.

The offset frequency Δ-Σ modulator is simply implemented by shifting fractional frequency. Carrier frequencies with fractional frequency already located outside the loop filter may just stay where they are. Otherwise, the fractional frequency can be relocated outside the loop bandwidth by simply adding/subtracting half of the reference frequency to the input of Δ-Σ modulator. As shown in Fig. 11(a), if fractional frequency ($f_{\rm fract} = Kf_{\rm ref}$) is smaller than the loop bandwidth ($f_{\rm lbw}$), or $f_{\rm fract} < f_{\rm lbw}$, $0.5\cdot 2^{21}$ will be added to the modulator input. On the other hand, if $f_{\rm fract}$ is larger than $f_{\rm ref} - f_{\rm lbw}$, $-0.5\cdot 2^{21}$ will be added to the modulator input. As shown in Fig. 11(b), fractional frequencies originally located inside the loop filter (i.e., the white box) are now relocated to center between two integer-divided frequencies (i.e., the gray box). Consequently, the associated fractional spurs can now be rejected effectively with the loop filter. A second order loop filter which typically rolls off 40 dB per decade is utilized to reject fractional spurs.

C. Half-Modulus Frequency Divider

To compensate for the frequency shift, the modulus divider must be switched concurrently to the half-modulus divider. The half modulus dividing function can be realized by bisecting the time interval of dividing either $2N+1$ or $2N-1$ in Fig. 12(a). It is fulfilled by re-sampling the modulus divider output with multi-phase signals generated from the VCO or subsequent divide-by-two circuit outputs. To shift $+f_{\rm ref}/2$, we use a 180° phase-delayed signal to sample the divider output. This can be accomplished by alternately sampling $N^{\rm th}$ cycle with a 180° phase signal and the $N+1^{\rm th}$ cycle with the 0° phase signal. Similarly, shifting $-f_{\rm ref}/2$ can be realized by alternately sampling the $N-1^{\rm th}$ cycle with 180° phase signal and $N^{\rm th}$ cycle with the 0° phase signal. The phase compensation sequence is shown in Fig. 12(b). The results are exhibited in Fig. 12(c), where frequencies in the gray box are shifted back to original frequencies while the fractional spurs remain and stay low. Prior arts have been demonstrated to implement fractional-N synthesizers using oscillators with multi-phase signals [12] or divide-by-two circuit [13]. But all suffered from fractional spurs due to multi-phase errors. Although sampling the divider output with differential phases also introduces spurs, they appear only at $f_{\rm ref}/2$, far from $f_{\rm lbw}$, since the phase error occurs only periodically during every other cycle.

Simulation in Fig. 13 indicates fractional spurs of -85 dBc/Hz in phase noise or -45 dBc in actual power over the 10 KHz resolution bandwidth. Timing-induced non-linearity is attributed to circuit distortion, primarily caused by supply and ground bounces. Usually, it is a slow varying function over time with substantially reduced higher harmonic spurious tones. At least 20 dB fractional spurs reduction is simulated by employing the offset-frequency technique until spurs are buried by the noise floor. Fractional spurs are actually shifted about 10 MHz in frequency. In addition, by assuming

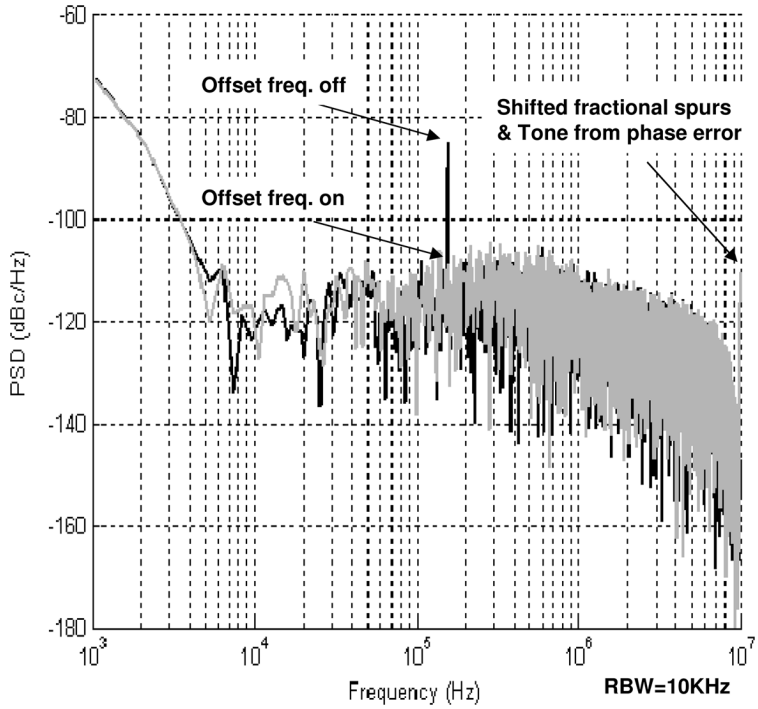


Fig. 13. Fractional spurs simulation comparison with/without offset-frequency technique.

10% differential phase error in re-sampling, an obvious tone is simulated near 10 MHz as well. In fact, both of them will be rejected by the loop filter.

IV. Circuits Implementation

The multiband synthesizer is based on a VCO core operating from 3.2–4 GHz [14]. The VCO output is divided by 2 to form the 1.6–2 GHz LO signal for the PCS/DCS band and mixed up to form the 4.8–6 GHz LO signal for 802.11a. The 2.4–2.5 GHz and 0.8–1 GHz LO signals for 802.11bg and cellular bands can be generated by adding divide-by-two circuits after the 4.8–5 GHz and 1.6–2 GHz LO signals in Fig. 1.

A. Wideband VCO Design

In wireless communication, VCO usually employs high-Q LC resonator to suppress the phase noise. The inductor is implemented on-chip with the spiral differential structure and its model is verified in SONNET software. The capacitor is designed tunable to change VCO frequency. Since high VCO gain results in high noise, a small varactor with a series of digitally-controlled switching capacitors are utilized to cover the wide frequency range. The switching device width, W, is traded off between the capacitor Q factor and tuning range because larger W has lower on-resistance but higher parasitic capacitance. The switching device length, L, limited to the feature size, can be further reduced by connecting two capacitors across the resonator in Fig. 14. The differential property will enable the virtual ground inside the device, and reduce the channel length and on-resistance to half. Two NMOS devices are cross-coupled to form a positive feedback to oscillate. Second LC resonant tank at the bottom is added for noise filtering [15]. Current tails are implemented with PMOS devices due to its lower flicker noise.

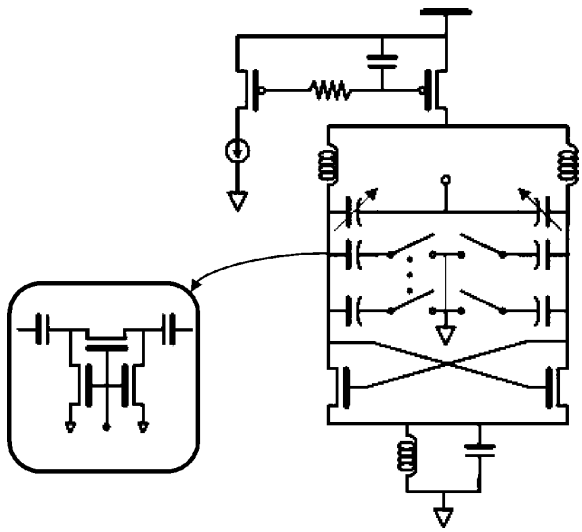


Fig. 14. Schematic of VCO with switching capacitors.

The RC filter at the gate of the current tail filters the noise contribution from current mirror devices and isolates supply noise by keeping V_{gs} constant.

B. Modulus/Half-Modulus Divider Design

Modulus divider is implemented with cascaded dual-modulus dividers [16], which divide the input frequency by 2 or 3. Six cascaded stages achieve modulus division from 64 to 127. To avoid the modulus dependent divider delay, the output of the modulus divider is sampled by the divide-by-two circuit subsequent to VCO. For the option of half-modulus divider, the sampling clock can be selected from differential phases of the divide-by-two circuit, in Fig. 1. It is also noted that the first three

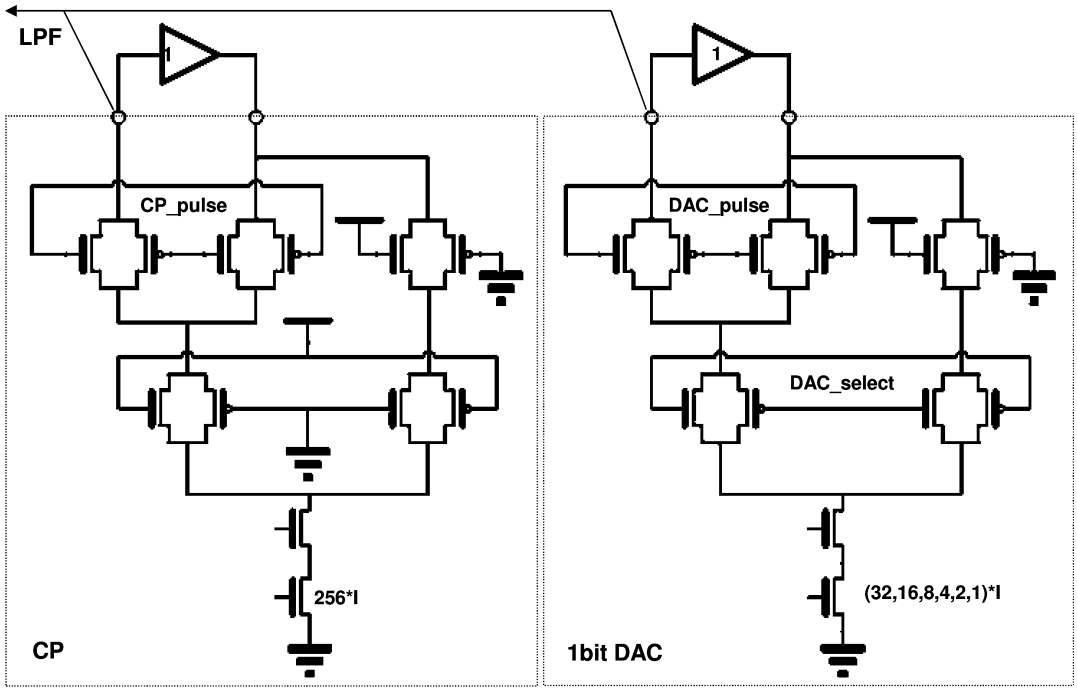


Fig. 15. Schematic of DAC and charge pump sinking currents.

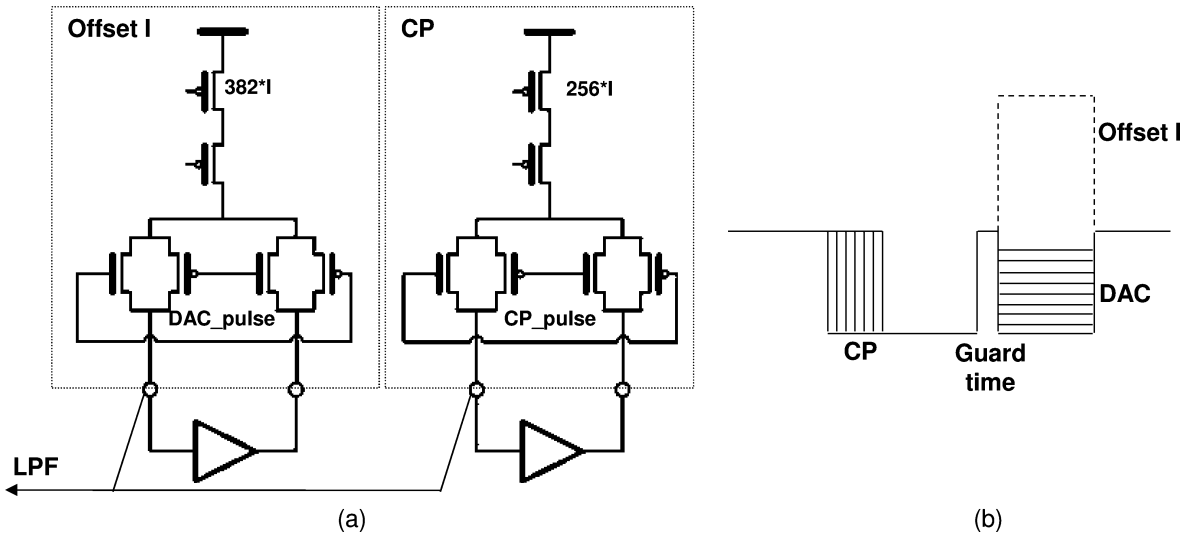


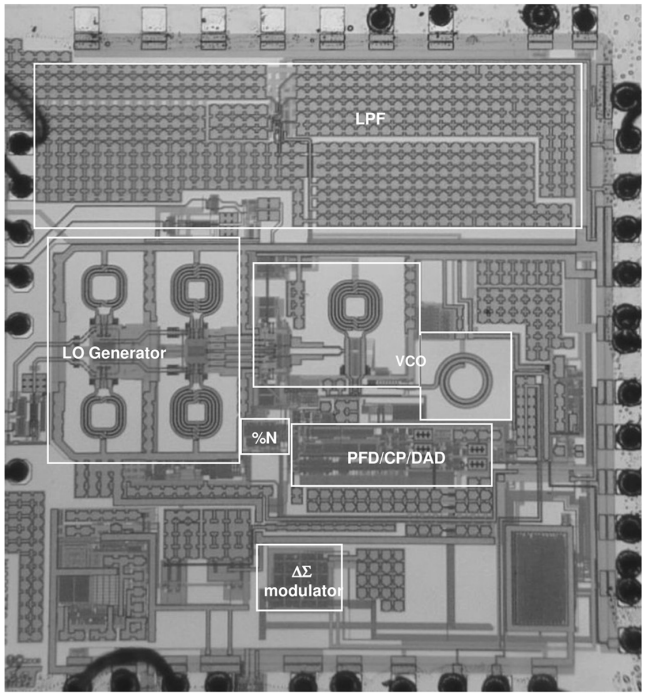
Fig. 16. (a) Schematic of offset and charge pump sourcing currents. (b) Timing diagram of charge pump and DAC.

stages are implemented with true single-phase clocked logic due to the speed requirement. The modulus/half-modulus divider is driven by a 4-bit MASH-111 output.

C. DAD and Charge Pump Design

Four 6-bit binary-weighted DACs are used to implement second order DAD with the pulse width equal to 4 times the output period of the divide-by-two circuit, 4 $T_{\mathrm{vco}/2}$, which is the trade-off between minimizing transient currents and noise. The output of PFD is converted to differential signals to drive the charge pump for better immunity from supply or ground bounces. By adding an offset current, only sinking currents are responsible for modulation in both charge pump and DAC. DAC replicates the charge pump to ensure the current matching in Fig. 15. The ratio of NMOS currents tail devices between DAC LSB and CP is 1:256. The LSB current of DAC is 3.9 uA with $W/L = 2.5$ um/3 um to minimize the power consumption and current mismatch over the process variation. The sourcing circuit of the charge pump and offset current are implemented with PMOS with no linearity requirement in Fig. 16(a). The voltage of the dummy terminal follows the loop filter output to avoid the transient voltage during switching. Fig. 16(b) shows the timing diagram of the charge pump, DAC and offset current pulses. A guard time is included to avoid charge pump transient current leaking to DAC.

The chip area is 4 mm^2, mostly occupied by LO generators, on-chip loop filters and pads, as shown in Fig. 17(a). The



(a)

Die photo 2x2 mm²		
	Area (mm²)	Current (mA)
VCO	0.25	8
LO generator	0.30	25
PFD/CP/DAD	0.08	10
Modulus divider Re-timer	0.01	4
ΔΣ modulator	0.03	2

(b)

Fig. 17. (a) Die photo; (b) Area and current consumption of key building blocks.

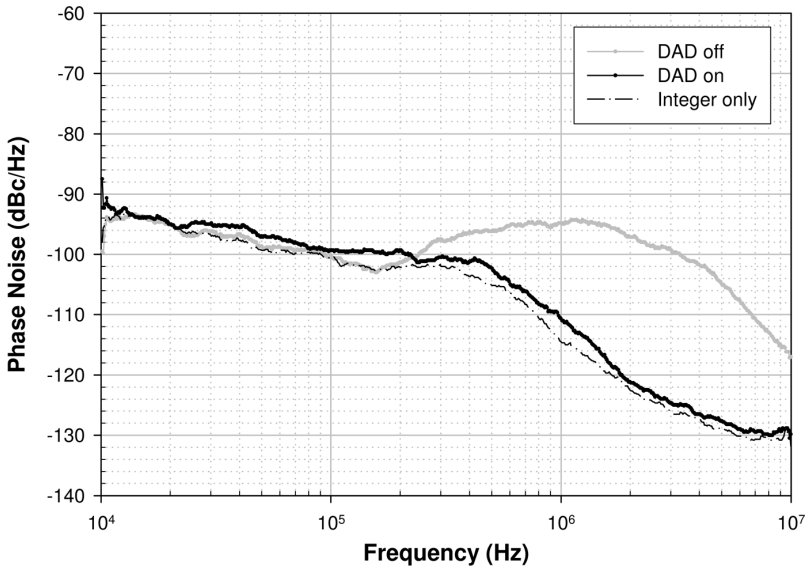


Fig. 18. Phase noise measurement with/without DAD at 3.24 GHz.

PFD/charge pump/DAD only occupies 0.08 mm^2 and the modulus divider with Δ-Σ modulator occupies another 0.04 mm^2. The total power consumption is 88.2 mW under 1.8 V supply. Excluding LO generators, the fractional-N PLL core consumes 24 mA, as shown in Fig. 17(b).

V. Measurement Results

A prototype 0.8–6 GHz fractional-N synthesizer chip is fabricated in 0.18 um CMOS process to prove the proposed techniques for quantization noise cancellation and fractional spurs reduction. Proper numbers of digital capacitors are selected so that VCO can operate at 3.24 GHz with the control voltage close to 1 V. The VCO gain is about 100 MHz/V, high enough to cover all the frequencies between digitally-controlled switching capacitors and small enough to avoid supply pushing. The phase noise is measured by HP spectrum analyzer 8563E. When the fractional number, K, is set to 0, the measured in-band noise is -100 dBc/Hz in Fig. 18. When K is set to 0.25, the synthesizer starts operating in fractional-N mode and the quantization noise rises significantly. After we enable the second order binary-weighted DAD, the quantization noise is greatly reduced

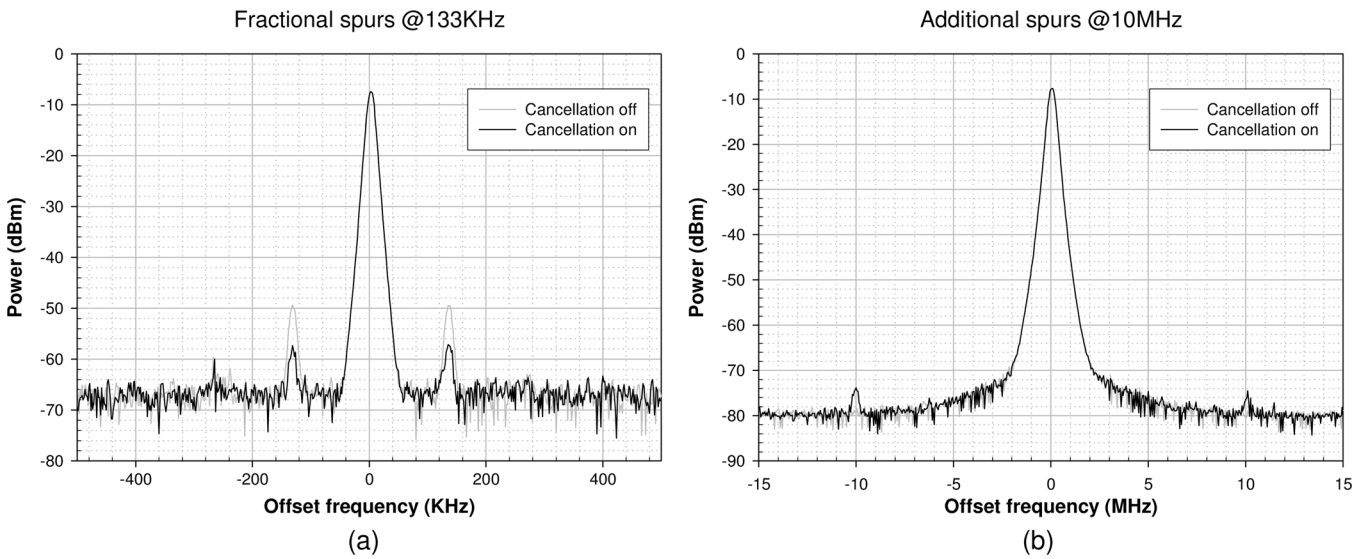


Fig. 19. Fractional spurs with/without cancellation at (a) 133 KHz and (b) 10 MHz.

TABLE I
PERFORMANCE SUMMARY

	Cellular	PCS/DCS	802.11bg	802.11a
Spot phase noise @100KHz (dBc/Hz)	-108	-103	-99	-92
RMS phase noise 10KHz~10MHz (degree)	0.25	0.38	0.58	1.28
Fractional spurs (dBc)	-50	-43	-50	-44
Reference spurs (dBc)	-71	-64	-67	-62

TABLE II
COMPARISON OF KEY SPECIFICATIONS TO THE STATE-OF-THE-ART

	This work	[1]	[2]	[3]	[5]
Frequency (Hz)	3.24G	2.1G	2.4G	3.6G	2.4G
Frequency Bands	4	1	1	1	1
Core Power (mW)	43.2	28	67	110	27.1
Core Area (mm^2)	0.37	N/A	1.53	2.7	N/A
Phase noise @100KHz (dBc/Hz)	-100	-104	-96	-98	-103
Fractional spurs (dBc)	-50	-60	-54	-45	-70
Noise suppression (dB)	25	15	16	29	N/A

by 25 dB at the MHz range. Compared with the integer-N operation, the phase noise is only 3 dB higher. Decreasing the loop bandwidth can further reduce the phase noise from quantization noise at expense of increasing VCO phase noise in band. This trade-off makes 400 KHz the optimal loop bandwidth with minimum integrated phase noise.

When K is set to 0.066, the high power density tones will appear at 133 KHz offset as high as -42 dBc in Fig. 19(a). The power of fraction spurs is not affected whether dithering is enabled or disabled. After enabling the offset-frequency technique, 8 dB reduction is observed. Second harmonic tones are also shown in the spectrum but 10 dB lower than fundamental tones. The additional spurs from re-sampling appear at 10 MHz offset, 66 dBc below the main tone in Fig. 19(b). Fractional spurs remain constant across all fractional numbers within the designed loop bandwidth. Remaining spurs are induced by the contaminated reference frequency jitter from the modulus divider ground bounce as explained in Fig. 7. It can be observed lowering the supply voltage of the modulus divider can greatly reduce fractional spurs. These coupling effects can be avoided by separating grounds with guard rings or employing differential signaling. By designing differential modulus divider, or oscillator buffers, fractional spurs can be further reduced.

The summary of the performance for different wireless standards is listed in the Table I. The in-band phase noise is determined by measuring spot phase noise at 100 KHz and the total phase noise is measured by integrating phase noise from 10 KHz to 10 MHz. Both phase noise and fractional spurs decrease linearly with the carrier frequency. However, fractional spurs in PCS/DCS and cellular bands do not drop as the carrier frequency scales because the offset-frequency technique is disabled during the measurement. Fractional spurs for PCS/DCS and cellular bands could be suppressed at least 8 dB more, if the offset-frequency technique were applied. The reference spurs are shown at 20 MHz and highly attenuated by the loop filter. Compared with previous published state-of-the-art PLLs, the proposed techniques consume substantially lower core area with relatively low power consumption without DEM and achieve competitive performance as shown in Table II.

VI. Conclusion

A compact 0.8–6 GHz fractional-N frequency synthesizer covering IEEE 802.11abg, PCS/DCS and cellular band is presented in this work. Two techniques are proposed to cancel quantization noise and reduce fractional spurs in the Δ-Σ modulator fractional-N PLL. First, MASH-111 Δ-Σ modulator with cascaded differentiators has eliminated digital processing blocks for noise-cancellation signal generation. second order binary-weighted DAD achieves second order mismatch shaping and reduces the quantization noise by 25 dB. It also has advantages of compact circuit implementation with smaller routing area and less power consumption over those of dynamic element matching (DEM) based counterparts. Second, third order offset-frequency Δ-Σ modulator reduces in-band spurs by 20 dB in simulation and 8 dB in present single-ended practice. The concept to shift the fractional spurs out-of-band has relaxed the charge pump linearity requirement. Fractional spurs caused by coupling effect are also identified and the differential signaling is suggested to improve the isolation for future implementations.

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