A Single-LC-Tank 5-10 GHz Quadrature Local Oscillator for Cognitive Radio Applications

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***Abstract* — This paper presents a local oscillator (LO) that converts oscillation frequencies of 13.3-20GHz from a single-LC-tank VCO to the intended 5-10GHz with continuous frequency coverage. A 4-stage differential injection-locked ring oscillator (ILRO) is used after the latch-based divider to produce quadrature output phases without requiring 50% duty cycle of input signals as those of conventional divide-by-2 approaches. When implemented in 65nm CMOS, the prototype LO consumes 22mA at 1V supply and is able to exhibit a worst-case phase noise of -102dBc/Hz at 1MHz offset across the entire 5-10GHz band for projected cognitive radio applications.**

***Index Terms* — CMOS, Cognitive Radio, Injection-locked ring oscillator, LC-VCO, Quadrature Phase Local Oscillator.**

I. Introduction

Cognitive radio (CR) is the latest contender for better spatial and temporal spectrum usage across an extensive frequency range, which is about 50MHz to 10GHz. In the foreseeable future, the widely used heterodyne radio architecture is more feasible, in terms of power and cost effectiveness, than direct sampling of the entire band by using A/D converters. Since the main functions of CR RF transceiver, including spectrum sensing, reception and transmission, may operate independently at different channel frequencies, multiple local oscillators (LOs) are needed for a system-on-chip (SoC) solution. In addition to the general LO requirements of low phase noise/spurs, quadrature output signals with 50% duty cycle, LO design for CR applications also requires compactness and low power dissipation, which are the two major emphases of this work.

In traditional wide bandwidth LO designs, LC-VCO often demands large silicon area, due to the need of large on-chip passive inductor and capacitor arrays, which are irreplaceable for low phase noise performance. It is therefore essential to find a compact circuit solution with only single-LC-tank to cover the entire CR band.

It is generally accepted once an oscillator has larger than 100% frequency tuning ratio (FTR) that is defined as

$$FTR=f_{max}/f_{min}-1 \quad (1)$$

all quadrature signals with frequencies lower than f_{min} are then obtainable by cascading multiple divide-by-2 circuits as needed. Accordingly, the required LO frequency range to cover the entire CR band from 50MHz to 10GHz can be condensed to 5-10GHz. Prior publications have reported greater than 100% FTR from a single-tank-VCO at lower frequencies [1]. Nonetheless, their achievable FTRs often depend greatly on process variations, which render reliable broadband RF products today using either multiple VCOs or a single VCO with subsequent frequency extension circuits.

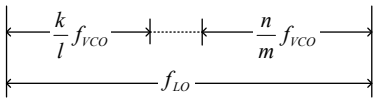

Fig.1. Concept of frequency extension (k, l, n, m are integers)

The basic principle for frequency extension is to multiply or divide VCO frequencies by variable integers or fractions, as shown in Fig.1. Two primary approaches were the programmable Miller feedback dividers [2] or the latch-based dividers. The former may introduce higher spur levels caused by unwanted mixer sidebands; the latter is usually preferred due to lower output spurs but can only generate signals with 50% duty cycle when the division ratios are even numbers.

To alleviate such shortcomings, we here present a both compact and energy-efficient 5-10GHz quadrature LO enabled by a novel frequency extension solution that takes full advantage of the natural characteristic of differential injection-locked ring oscillator (ILRO) for producing the needed quadrature outputs with 50% duty cycle.

The following Section II addresses detailed issues in relevance to existing quadrature generation approaches and offers differential ILRO as a superior solution for both performance and area/power consumption. Section III describes LO architecture and relevant circuit schematics. Section IV presents test results from an implemented LO in 65nm CMOS. Finally in Section V, we summarize the overall development work.

II. Differential ILRO as Quadrature Signal Generator

The design of an LO with adequate frequency extension must first ensure the generation of quadrature output signals with 50% duty cycle.

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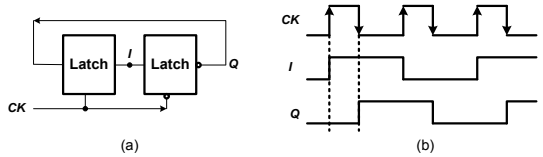

Fig.2. (a) Divider-by-2 circuit and (b) Quadrature phases generated from input edges

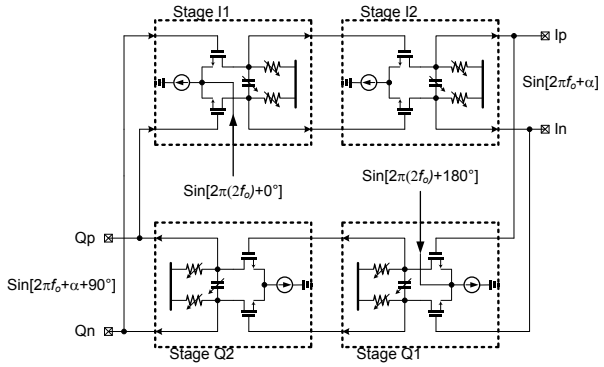

Fig.3. A 4-stage differential ILRO

Several major types of solutions have been suggested in the past, including: 1) Poly-phase filters, which have significant signal attenuation and thus inadequate for CR applications; 2) Quadrature oscillators with multiple LC-tanks, which are inherently large in size [3]; 3) Divide-by-2, which is generally good for compact circuit design, but would introduce two major challenges, including: a) Since it performs frequency division, all preceding stages, i.e. VCO and frequency extension circuits, must operate at twice higher frequency than desired. Or as an alternative, a frequency doubler must be inserted before the divide-by-2. In either case, it will lead to higher power consumption; b) As shown in Fig.2, it mandates input signals to maintain 50% duty cycle and any deviation from it will lead to output phase mismatch according to Eq.2,

$$\Phi_{\text{mismatch}}=|Input\_Duty\_Cycle\times 180°-90°| \qquad (2)$$

However, when odd division ratios are chosen, output signals of programmable dividers for frequency extension can hardly retain 50% duty cycle, unless complex and power hungry duty cycle correction circuits are also used.

To avoid disadvantages from previous quadrature generation approaches, we now propose to use a differential ILRO as the quadrature phase output generator. As indicated in Fig.3, it contains only four delay cells to assure accurate quadrature phase outputs and the least restriction to high frequency operation.

Each delay cell in ILRO contains a differential pair that has variable RC load for maximizing the locking range. The input signal is injected differentially to the common nodes of differential pairs in stage I1 and Q1 in Fig.3.

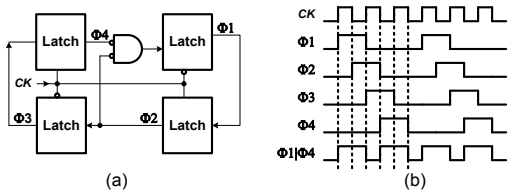

Fig.4. (a) Divider-by-3 circuit and (b) waveforms

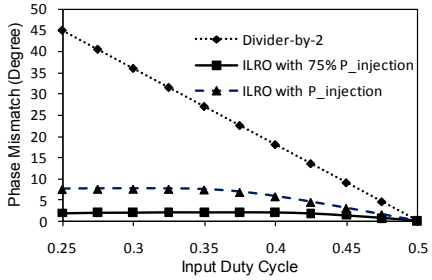

Fig. 5. Output quadrature phase mismatch vs. input duty cycle

The output frequency would only be one half of the input frequency under the locking condition, which is similar to that of a divide-by-2 operation. However, the preceding programmable divider often gives two signals that can be combined by a logic gate to double the output frequency. Take the divider-by-3 in Fig.4 as an example: both Φ1 and Φ4 have 33% duty cycle, and they can double the input frequency through logic OR operation. In the proposed ILRO, such a logic gate can be embedded into bias circuits without consuming additional current, which simplifies the design and saves energy.

ILRO possesses additional superior characteristics for quadrature signal generation:

1. Its quadrature output phase mismatch is not a strong function of its input duty cycle. This is fundamentally different from a typical divide-by-2 circuit. To illustrate it qualitatively, Fig.5 shows simulated phase mismatches of different quadrature generation methods versus the input signal duty cycle. As indicated, ILRO's phase mismatch is significantly lower than that of divide-by-2 when input duty cycle deviates from 50%. It also indicates ILRO's less dependence on input signal injection power.
2. Fig.5 also indicates that, if needed, phase mismatch can be further reduced by less injection power.
3. With differential delay cells, ILRO can generate 50% duty cycle naturally and is strongly immune to common mode interferences.
4. When locked, ILRO exhibits phase noise of a driven circuit rather than an autonomous one. Therefore, LO's overall phase noise is still dominated by the VCO, not ILRO [4].

In summary, using ILRO for generating quadrature phase outputs would greatly simplify the frequency extension circuit design and thereby decrease its power consumption. Further details on circuit designs will be discussed in the next section.

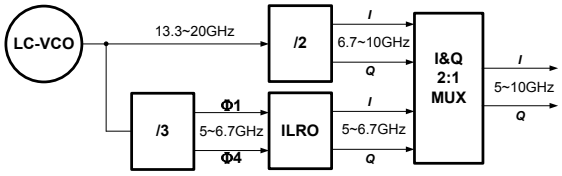

Fig. 6. Architecture of 5~10GHz quadrature LO

III. Design of 5~10GHz Quadrature LO

We start the LO frequency planning by using a 50% FTR VCO which can oscillate from 13.3 to 20GHz. Consequently, a 5-10GHz LO is designed in Fig.6 with a divide-by-2 after LC-VCO to produce 6.67-10GHz quadrature signals with a 50% duty cycle and by using a parallel divide-by-3 to produce 5-6.67GHz quadrature phase output signals with 33% duty cycle as shown in Fig.4. We then feed the divide-by-3 output through the proposed 4-stage differential ILRO which consists of an embedded frequency doubler to generate desired 50% duty cycle quadrature signals. Under such arrangement, the ILRO is also relaxed to cover only 25% of FTR.

The building block design will be described as follows.

A. VCO and Buffer

Fig.7 shows the LC-VCO schematic with an output buffer. The LC tank consists of one 0.24nH differential inductor, a pair of AC-coupled accumulation mode NMOS varactors that can be tuned differentially for the maximum variable capacitance and seven additional pairs of DC coupled switchable NMOS varactors to cover 8 frequency bands with overlaps.

On the other hand, the inverting buffer for Vtune converts single-ended control voltage to differential ones. Its voltage curve is flatter in the middle region and sharper at the extremes. With this characteristic, this voltage converter not only extends the linear region of varactor's C-V curve, but also reduces its noise contribution to the VCO.

B. Frequency Dividers and Multiplexers

Fig.2 and Fig.4 illustrate the circuit structure of divide-by-2 and 3. The latch, AND gate and multiplexer used in the frequency extension circuit are all designed in current mode logic (CML). Each of them possesses 250Ω load resistors and consumes about 1.4mA under 1V supply voltage.

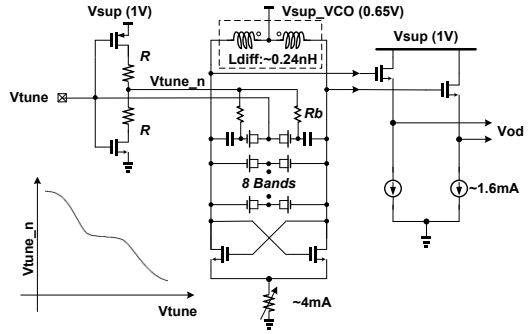

Fig. 7. Simplified schematic of VCO and buffer

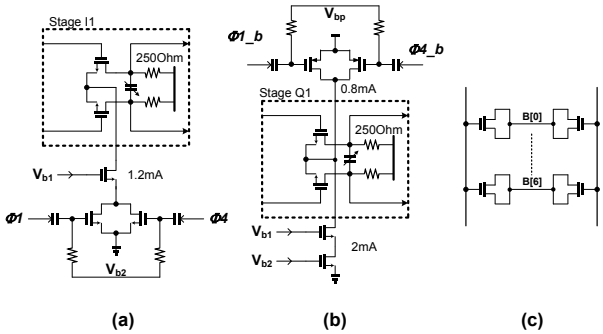

Fig.8. Schematic of ILRO (a) Stage with embedded NMOS OR gate (b) Stage with embedded PMOS OR gate (c) Switchable NMOS varactors in the load for variable self oscillation frequencies

C. Injection-Locked Ring Oscillator

The overall differential ILRO topology is provided in Fig.3, with Fig.8(a) showing the specific stage with embedded NMOS OR gate that combines Φ1 and Φ4, and Fig.8(b) showing the specific stage with PMOS OR gate that combines Φ1_b and Φ4_b. These two OR gates can produce differential injection signals at the twice of the input frequency.

Seven switchable NMOS varactors, each with 10fF at 0V bias voltage shown in Fig.8(c), are designed to provide 8 evenly distributed self-oscillation frequencies covering from 5 to 6.7GHz, which also relaxes the needed injection level for locking purpose, hence minimizing the quadrature phase mismatch.

IV. Prototype and Measured Performance

A prototype LO has been implemented in 65nm CMOS. As shown in Fig.9, it contains a 5-10GHz quadrature LO (Fig.6), a divide-by-4 and a differential to single-ended buffer for both I and Q channels. The VCO and buffer occupy a total area of 350x250um^2, and the frequency

extension circuit, including divide-by-2 and 3, ILRO and multiplexers, occupies 130x150um^2.

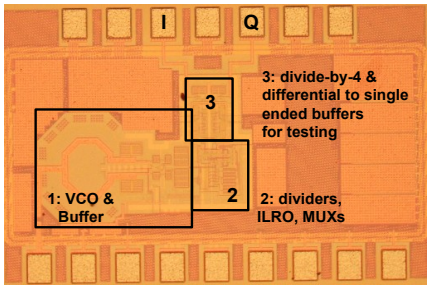

Fig.9. Die photograph

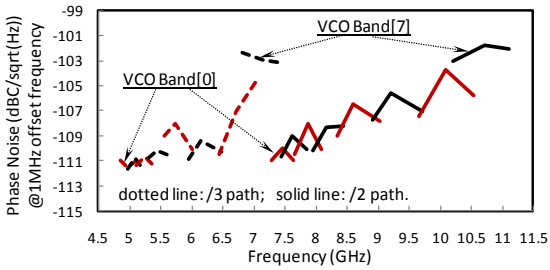

Fig.10. Phase noise vs. LO frequency (Note: 12 dB is added to the overall measured LO phase noise profile to cancel the effect from divide-by-4 circuit embedded in the test driver)

Fig.10 plots the LO frequency coverage and phase noise at 1MHz offset frequency. Each line segment on the chart represents a VCO band with 0.1~0.9V tuning voltage. The VCO actually covers 14.6-22.3GHz (a 53% FTR), which is higher than simulated results. LO actually covers 4.8-11.1GHz after the frequency extension. With the same VCO band, divide-by-3 path generally exhibits less phase noise than divide-by-2 path, which confirms that the locked ILRO contributes less noise than VCO.

When ILRO is locked at the 6.44GHz, Fig.11 shows the output phase noise profile and spectrum, which contains higher order harmonics but no visible spurs.

Measured LO quadrature phase mismatch is about 2° and 3~4° for divide-by-2 path and divide-by-3 path respectively, which is acceptable by most RF systems today [5].

V. Conclusion

This paper presents a quadrature LO with 5-10GHz continuous frequency coverage by using a single-LC-tank VCO with differential ILRO as the quadrature phase output generator. The worst-case phase noise is measured as -102dBc/sqrt(Hz) at 1MHz offset frequency. When implemented in 65nm CMOS, it occupies less than 0.11mm^2 silicon area and consumes 22mA at 1V power supply when divide-by-3 and ILRO path is activated.

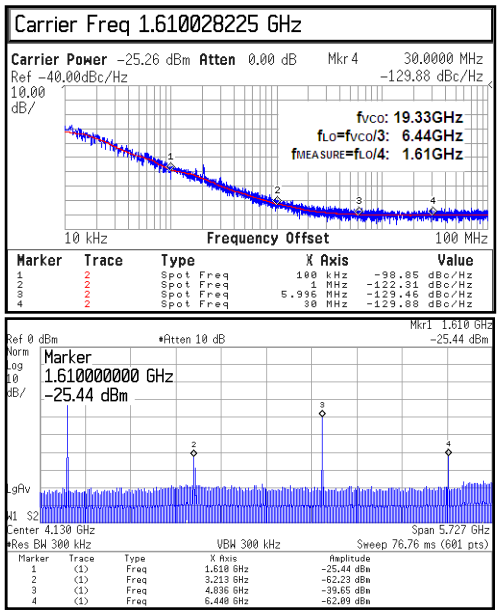

Fig.11. Phase noise profile (upper) and output spectrum (lower) when ILRO is locked at 6.44GHz

Compared with the state-of-the-art [3] that produced 1-10GHz quadrature LO, this work lowers the worst case phase noise by about 7dB and saves the silicon area by more than 50%. It also saves power consumption by 33%, without counting the power of the two divide-by-2 circuits that are needed to extend the LO frequency down to 1.25GHz range, which is about 2-3mA by estimation.

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References

[1] A. Berny,et al., "A 1.8-GHz LC VCO With 1.3-GHz Tuning Range and Digital Amplitude Calibration", IEEE J. Solid-State Circuits, vol. 40, no.4 pp.909~917, Apr. 2005.

[2] Y. Ito, et al., "A 0.98 to 6.6 GHz Tunable Wideband VCO in a 180nm CMOS Technology for Reconfigurable Radio Transceiver", IEEE Asian SSCC. Dig., pp.359-362, 2006.

[3] B. Razavi, "Multi-Decade Carrier Generation for Cognitive Radios", *IEEE VLSI Circuits, Symp. Dig*., pp. 120-121, June 2009.

[4] S. Verma, et al, "A Unified Model for Injection-Locked Frequency Dividers", IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 1015-1027, Jun. 2003.

[5] Q. Gu, "RF System Design of Transceivers for Wireless Communications", Springer, 2005.