A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c Transceiver

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***Abstract*—A low phase noise, wideband, mm-wave, integer-N PLL that is capable of supporting an 802.15.3c heterodyne transceiver is reported. The PLL can generate 6 equally spaced tones from 43.2 GHz to 51.84 GHz, which is suitable for a heterodyne architecture with $\mathrm{F_{LO}} = (4/5) \times \mathrm{F_{TRX}}$. Phase noise is measured directly at the $\mathrm{F_{LO}}$ frequency and is better than −97.5 dBc/Hz@1 MHz across the entire band. The reported frequency synthesizer is smaller, exhibits less phase noise, and consumes less power than prior art. In addition, the $\mathrm{F_{LO}}$ tone corresponds to the fundamental of the VCO as opposed to a higher harmonic.**

Central to the PLL performance is the design of a low-noise, wideband, mm-wave VCO with a 22.9% tuning range. Fine discrete tuning and minimization of parasitics is achieved using a programmable transmission line as a frequency tuning element.

***Index Terms*—60 GHz, mm-wave, phase noise, PLL, VCO, wideband.**

I. Introduction

THE past few years have seen a dramatic rise in the number of mm-wave publications targeting the unlicensed 57–66 GHz spectrum. This is with good reason: The unprecedented amount of available bandwidth should facilitate the emergence of a host of new products that utilize this band for short range, exceptionally high speed, wireless transmission. Sub-micron CMOS has already demonstrated adequate performance at these frequencies and, so, given well known semiconductor trends, will inevitably establish itself as the technology of choice for low-cost, high volume 60 GHz products [1].

Current standard governing wireless communication at 60 GHz are typically based on the IEEE 802.15.3c specification [2], which divides the band into four distinct channels with centre frequencies ranging from 58.32 GHz to 64.8 GHz (Fig. 1). Modulation rates and schemes vary, but each channel should permit transmission rates of at least 2 Gbit/s up to a distance of about 10 meters. Naturally, any transceiver (TRX) that is to be standard compliant requires a circuit to synthesize each of these carrier frequencies. As only four distinct tones are required, the integer-N PLL topology is sufficient, however, as in all mm-wave research, the challenge lies in the design of the blocks operating at very high frequencies, namely the VCO, buffer and dividers, which all require an output-referred tuning range in excess of 7 GHz. Moreover, as systems move away from single-carrier modulation and adopt more complex schemes (such as OFDM), achieving good phase noise performance coupled with wideband tuning will become increasingly necessary and challenging. Within this context, we present a low noise, integer-N PLL that is capable of supporting a heterodyne 802.15.3c TRX where the receive/transmit frequency $(\mathrm{F_{TRX}})$ is 1.25 times the main synthesizer tone $(\mathrm{F_{LO}})$ and 5 times the intermediate frequency $(\mathrm{F_{IF}})$, i.e., $\mathrm{F_{TRX}} = (5/4) \times \mathrm{F_{LO}} = 5 \times \mathrm{F_{IF}}$ [3].

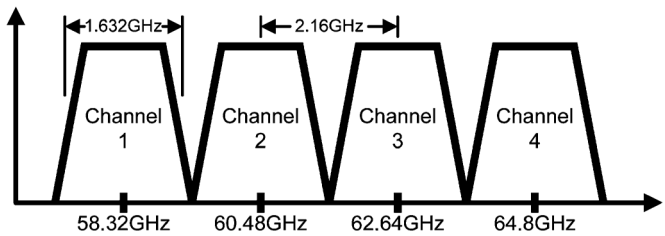

Fig. 1. The IEEE 802.15.3c channel specification.

Previous work has already demonstrated the feasibility of CMOS mm-wave synthesizer design. In [4], the authors used injection locking to reduce area and power while maintaining good in-band noise performance. Later, in [5], a synthesizer that generated quadrature outputs directly at 60 GHz with a 9 GHz tuning range was realized. Both these publications, however, report poor phase noise measurements for frequency offsets outside the PLL's loop bandwidth. More recent work has employed a quadrature-VCO running at 20 GHz and a push-push technique to isolate the second harmonic [6]. This work, which specifically targeted the IEEE 802.15.3c specifications, could cover three of the required four 60 GHz channels and demonstrated very good phase noise (−94 dBc/Hz@1 MHz normalized to Band 3). Despite good performance metrics, drawbacks to this approach exist: Quadrature oscillators add substantial design complexity and introduce issues such as the potential for uncertain mode behaviour and reduced quadrature accuracy. In addition, techniques that isolate the second harmonic typically provide poor drive strength or require power-hungry buffers prior to the down-conversion mixers. Compared to [6], we achieve a wider tuning range and lower phase noise using a VCO to directly generate the $\mathrm{F_{LO}}$ frequency. This simpler and more robust approach avoids the aforementioned issues.

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Central to this endeavour is the design of a wideband, mm-wave VCO. While standard RF design techniques can be applied to mm-wave designs, one should be aware of certain changes to the design paradigm. Most notably, resonator loss is typically determined by the quality of the capacitive-tuning elements rather than the inductor and, therefore, the choice and design of this tuning element has a large impact on the performance of the VCO itself. Moreover, while second-order effects such as tank loading and flicker noise up-conversion can dominate in any wideband CMOS VCO, the situation is even more deleterious in mm-wave oscillators, since it is difficult to realize a high impedance node at twice the oscillation frequency across the entire tuning range [7], [8]. The problem is further exacerbated if a single large varactor is used to cover the very wide tuning ranges typically demanded at mm-wave; the poor Q of CMOS varactors at mm-wave degrade the Q of the resonator, while the resultant large and nonlinear K_{VCO} values increase AM-to-PM conversion [9]. To minimize such effects, it is necessary to linearize the resonator as much as possible and limit the size of the varactor, which typically means introducing some form of digital tuning into the design [10]. Another important practical concern at mm-wave frequencies is routing parasitics, which can result in large discrepancies between simulation and measurement. To address these problems, this work utilizes Digitally-Controlled-Artificial-Dielectric (DiCAD) as a frequency tuning element in all mm-wave circuit blocks. DiCAD originated as a method to control the permittivity of a differential transmission line using CMOS switches [11]. When used in resonators, DiCAD is a useful technique that enables fine and linear digital frequency tuning, minimizes routing parasitics, and facilitates "first-time right" design [12].

As with many published mm-wave CMOS circuits, both lumped-element techniques and distributed-element techniques [13] have been successfully employed in mm-wave VCOs. Generally speaking, a purely lumped-element approach results in more compact designs, whereas a distributed-element approach results in better matching between simulation and measurement (transmission lines give more precise control over small reactances and interconnect wiring can be incorporated into the model [14]). The approach outlined in this work, specifically the use of DiCAD, can be viewed as a hybrid approach that uses a programmable transmission line to realize very fine resonator tuning while accurately modelling interconnect routing, but uses lumped-element design elsewhere to reduce area.

Section II introduces the choice of PLL topology and discusses the frequency plan of the TRX for which the PLL was designed. Section III discusses the advantages of using DiCAD as a frequency tuning element, while Section IV documents other key mm-wave design choices. Measurements are provided in Section V and conclusions are drawn in Section VI.

II. PLL Topology

The PLL described in this work was designed to support a heterodyne transceiver that employs separate, but identical PLLs for the receive and transmit paths (Fig. 2). A dual PLL solution was used to reduce the LO routing between the VCO buffer and the RF mixers, which can result in drive strength issues at 48 GHz. Referring to the receive path: The incoming 60 GHz signal (F_{RX}) is first down-converted through a single-phase 48 GHz tone (F_{LO}) to a 12 GHz intermediate-frequency (F_{IF}), before being down-converted again to the baseband through I/Q paths. While this architecture requires an anti-aliasing filter[1] to suppress the image and minimise noise-folding, it has the advantage of greatly relaxing the design of the frequency synthesizer. A direct conversion transceiver would require I/Q quadrature generation at 60 GHz, which would necessitate either a 120 GHz VCO, or a 60 GHz QVCO complete with many its shortcomings including: I/Q routing and accuracy issues, and potential uncertainty in mode selection. By contrast, the two-step (or heterodyne) approach requires only a single-phase 48 GHz VCO, while the 12 GHz I/Q signals are generated through a CML divider.

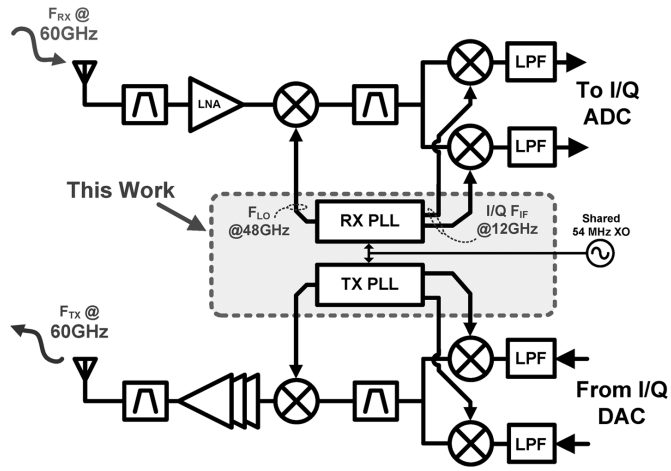


Fig. 2. A heterodyne 60 GHz transceiver with separate TX/RX PLLs.

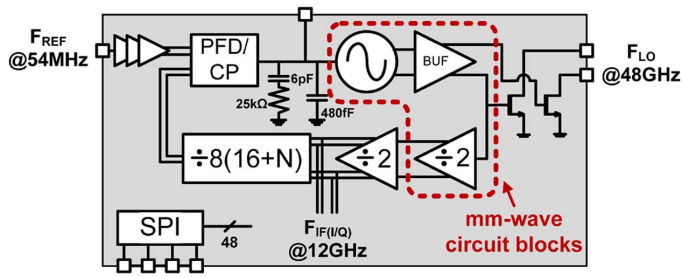


Fig. 3. The fabricated integer-N type-II 48 GHz PLL (with highlighted mm-wave blocks).

There is also some performance advantage to operating the VCO at 48 GHz as opposed to 60 GHz. As you move to higher frequencies, capacitor-Q degrades linearly with frequency, while inductor-Q *ideally* increases as a linear function of frequency. In CMOS technologies, however, inductor-Q's are typically limited by skin effects and substrate losses and,

[1]The LNA currently employs a tuned transformer-based resonator at its input, which also functions as bandpass filter and should give about −25 dB to −30 dB of suppression at the 36 GHz image frequency.

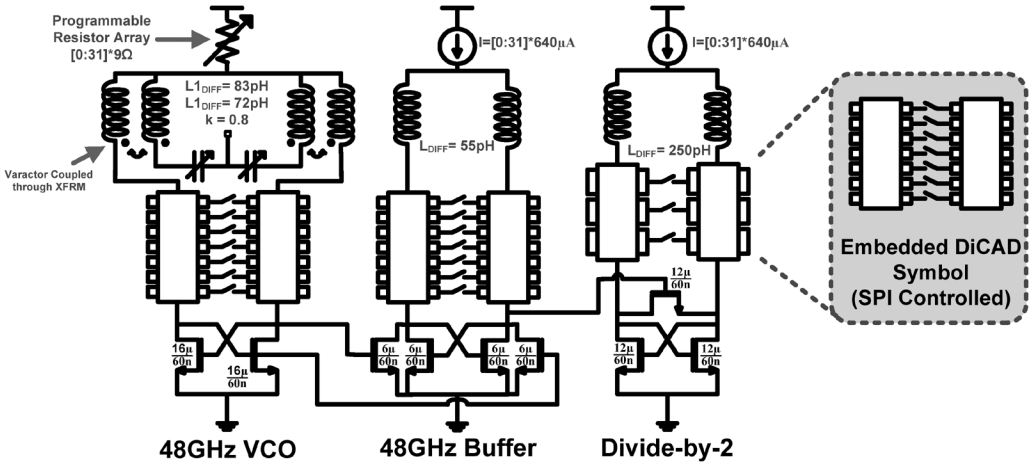


Fig. 4. Millimeter-wave circuit blocks used in the PLL. All blocks employ DiCAD as a frequency tuning element.

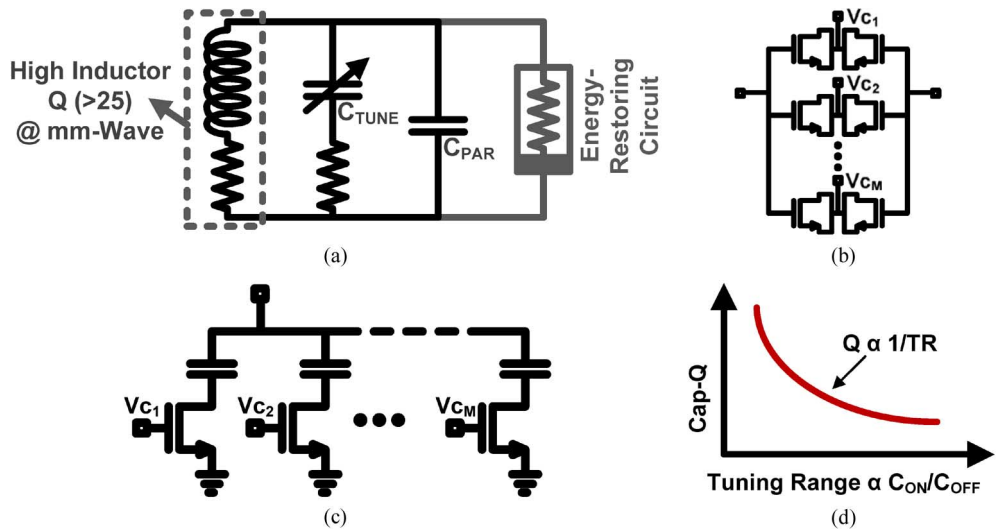


Fig. 5. An overview of possible frequency tuning schemes. (a) Simplified LC oscillator; wideband mm-wave VCOs are typically limited by loss associated with C_{TUNE}. (b) Digitally controlled varactor bank. (c) Switch capacitor bank is best option at RF, but interconnect reduces performance at mm-wave. (d) Q/TR trade-off of a switch cap array.

so, while there might be some benefit to operating a narrowband mm-wave oscillator at higher frequencies (in terms of oscillator figure of merit), it is deleterious for very wideband oscillators where capacitive tuning elements determine the resonator-Q.

The proposed programmable integer-N, Type-II, third order PLL is shown in Fig. 3. The focus of this work is the mm-wave blocks consisting of a DiCAD-based VCO, injection-locked buffer and injection-locked frequency divider (shown separately in Fig. 4). The rest of the divider chain consists of CML-based logic; a prescaler divides the 24 GHz divider output by 16 while also generating IQ phases at 12 GHz, and a multi-modulus divider further divides the signal by 16+N (where N is a 4-bit binary code). Using this scheme, any divide ratio from 512 to 992 in steps of 32 can be obtained. This divide ratio together with a 54 MHz reference enables synthesis of the required tones. A PFD, current-steering charge pump and second order on-chip loop filter complete the block. To increase flexibility during testing, the on-chip loop filter can be disabled and an off-chip loop filter can be employed.

III. Frequency Tuning Using DiCAD

In this work all the mm-wave resonators employ DiCAD as a digital frequency tuning element. Its origin, structure and advantages are outlined in this section.

1) The Motivation for DiCAD: A simplified lumped equivalent model of an LC oscillator is shown Fig. 5(a). Losses in the inductor and capacitive-tuning element as well as any equivalent positive resistance in the energy restoring circuitry will degrade the resonator's Q [15]. Compared to RF, inductor-Q's at mm-wave frequencies can be very good; in the process used in this work, i.e., a 6-metal layer process with an ultra-thick top metal layer (3.4 μm), it is possible to obtain Q's in excess of 25 at 48 GHz for a single turn inductor. Further, since Q-degradation due to transistors in the energy restoring circuit is hard to avoid but can be minimized, this work has focused on the design of the capacitive tuning element, which typically limits performance.

The simplest way to obtain the required frequency tuning is to use a single large varactor. This comes at the cost of a substantial

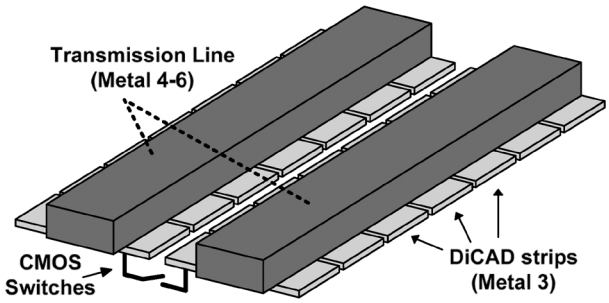


Fig. 6. The physical structure of Digitally-Controlled-Artificial-Dielectric (DiCAD); when all switches are closed, the structure can be viewed as a "slow-wave" transmission line [14].

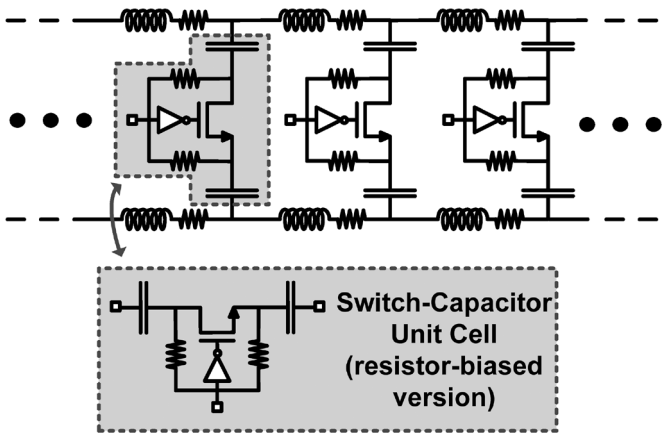


Fig. 7. The circuit equivalent model of DiCAD can be viewed as a distributed switch capacitor bank.

degradation in resonator-Q. Its large K_{VCO} value also results in a large up-conversion of flicker noise and, when employed in a PLL, a large up-conversion of noise from the charge pump and loop filter. The standard approach to minimizing these effects is to employ both discrete tuning and continuous tuning [10], where linear capacitors provide discrete tuning, and a small varactor (with an accompanying small K_{VCO} and reduced effective loss) provides continuous tuning. Such discrete-linear tuning can be realised using a bank of varactors, which are digitally controlled such that are always biased in their linear region (Fig. 5(b)). A better approach to use a bank of switchable capacitors (Fig. 5(c)), which exhibits an improved trade-off between Q and tuning range (TR); a large switch gives better Q, but a reduced C_{ON}/C_{OFF} ratio and vice versa [16] (Fig. 5(d)). While this approach works well at RF frequencies, it is problematic at mm-wave where interconnect traces contribute a significant portion of inductance and capacitance to the resonator, which can significantly shift the centre frequency. Accounting for all these traces, while possible [17], is difficult and becomes increasingly problematic at higher frequencies. To speed design times, one can always overdesign the switch capacitor bank with a large overlap between switch code and a large margin at either side of the band, but this unnecessarily reduces the resonator's Q and thus reduces the oscillator's figure of merit (FOM). The goal is therefore to realize a capacitive-tuning scheme that not only minimizes parasitics, but also accurately accounts for them.

2) DiCAD Structure: Early publications reporting CMOS 60 GHz circuits, had as much in common with discrete microwave design as it had with standard RF CMOS lumped-element design.[2] Quarter-wave resonators, transmission lines and inter-stage matching techniques were common. In an effort, to provide flexibility for such designs, the idea of DiCAD (or Digitally controlled Artificial Dielectric [11], [12]) was developed. DiCAD consists of a transmission line constructed from the top metal layers in a CMOS process, underneath which are placed metal strips (see Fig. 6). By placing a CMOS switch between these strips, the equivalent dielectric constant of the transmission line can be altered and thus its electric length can be changed. For our purposes, this structure can be viewed as a distributed capacitor array (Fig. 7) and, therefore, when used in an mm-wave VCO, DiCAD can reduce the varactor size (and K_{VCO}) in the same way as switched-tuning of a VCO [10], i.e., the DiCAD structure provides discrete linear tuning and, therefore, only a small varactor is needed to provide continuous tuning.

Using this structure as a frequency tuning element at mm-wave has a number of advantages:

- *It is easily modelled*: By importing the structure (with ideal open and shorts between the strips) into an electromagnetic (EM) simulator, the equivalent transmission line model in Fig. 7 can be obtained. Once the CMOS switches are included, it can be used in all circuit level simulations.
- *It is EM friendly*: The structure is very regular and results in short EM simulation times.
- *It eliminates/accounts for routing parasitic*: Routing parasitics are inherent in the structure and, so, are completely captured in the transmission line model. For instance, in our final VCO design, the differential inductance of the DiCAD with all switches open is approximately 34 pH. Given that the equivalent inductance of the rest of the resonator is only 83 pH, neglecting the effect of routing would create a significant difference between the simulated and measured oscillation frequencies.
- *It is accurate*: Each pair of DiCAD strips function as a capacitor, which in our design is calculated as approximately 3 fF differentially. Such small values allow us to sacrifice area (compared to MIM or finger caps), with reduced variability.

Embedding this structure into all the mm-wave resonators enables fine digital tuning (down to a few fFs) and "first-time right" design promised by distributed element design. Indeed, in the final design, the discrete tuning resolution was not limited by the DiCAD structure, instead excessively small steps were avoided in order to prevent the PLL falling out of locked due to frequencies variations arising from temperature or amplitude changes.

3) Switch-Selection: In the same way that a transmission line is schematically indistinguishable from its RLCG frequency dependant model, DiCAD is schematically indistinguishable from a distributed switched capacitor bank. Given this, its performance is fundamentally limited by the CMOS transistors in the equivalent switched-capacitor unit cell (Fig. 7). Two common switch-capacitor unit cells are shown in Fig. 8. The self-biased

[2]An interesting example is [18]. In the RX portion of that chip, transmissions lines are extensively used, whereas when the TX was designed, the authors favoured lumped passive element design.

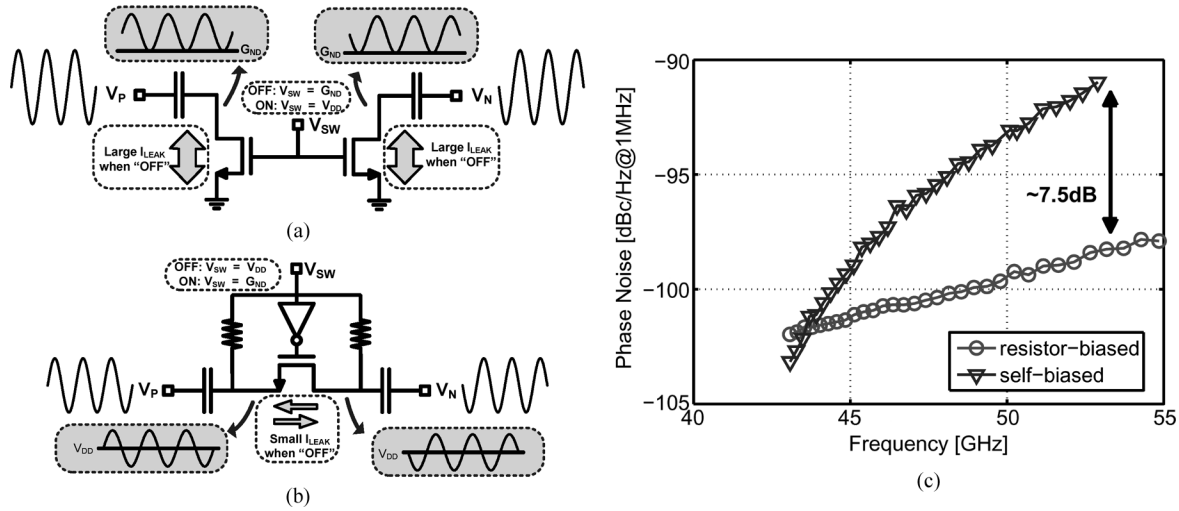


Fig. 8. A comparison of switches that can be used in the programmable transmission line. (a) Self-biased switch; (b) resistor-biased switch; (c) simulated phase noise.

switch (Fig. 8(a)) was used in the first realisation of a switched-tuning VCO [10]. The resistor-biased version (Fig. 8(b)) is also commonly used and has been shown to exhibit an enhanced Q and, thus, exhibits a better trade-off between tuning range and phase noise [16].

In addition, we have also observed a reduction in phase noise degradation due to drain-to-source leakage currents when the resistor-biased switch is used. Consider the self-biased switch: When the switch is in the OFF state, the oscillation waveform at the drain node is such that at the trough of an oscillation, the drain voltage briefly drops below the source. This causes the device to pull current from the ground. Under steady-state conditions, the amount of charge pulled from ground must equal the charge lost due to device leakage current. Noise associated with these currents can degrade the overall phase noise performance of the VCO. By contrast, the resistor-biased switch does not suffer from this effect; when OFF, both $\mathrm{V_{GS}}$ and $\mathrm{V_{GD}}$ of the transistor are biased around a large negative potential $(-\mathrm{V_{DD}})$ and, so, the amount of leakage current is greatly reduced. Fig. 8(c) shows simulation results for our finalized VCO, with both the self-biased and resistor-biased switches. As expected, when the switches are on, the performance is similar. However, when all 31 switches are off, the resistor-biased switch achieves a 7.5 dB improvement in phase noise. Using SpectreRF, it was deduced that this degradation was due to noise current flowing in the OFF switches. This mechanism is likely to be apparent only in deep-scaled general-purpose (GP) CMOS technologies where significant leakage currents are present, as opposed to the low-power (LP) CMOS process option.[3] Based on these simulation results, the resistor-biased switch was implemented in our design and sized such that the OFF capacitance was $\sim$1.3 fF while the ON capacitance was $\sim$3 fF.

[3]The choice of the GP process was guided by the LNA and PA design rather than the PLL design. The higher $\mathrm{F_T/F_{MAX}}$ should yield a performance boost in those blocks. The advantage of the GP process in terms of achievable VCO phase noise is more ambiguous; the GP process results in less parasitics for a given negative resistance, but it also necessitates a lower oscillation amplitude and increases Q-degradation due to reduced drain-source resistance in the differential pair.

IV. Key mm-Wave Design Choices

A central focus of this work has been on the design of mm-wave blocks shown in Fig. 4, since performance metrics of these blocks translate directly into important integer-N PLL performance metrics such as tuning range, power consumption, and phase noise. The remaining circuit blocks that operate at lower frequencies, while important, are well understood and have been extensively studied elsewhere.

1) mm-Wave VCO: The VCO was realized using the standard voltage-biased NMOS topology. Compared to the current-biased topology, the voltage-biased topology is known to result in Q-degradation of the resonator (explained in [7] and quantified in [15]). However, Q-degradation will also occur in current-limited topologies if the current source does not present a high impedance around the second harmonic [7]. For this design, this criterion would require a current source with a high impedance that is tunable from 86 GHz to 104 GHz. Given the difficulty of realising such a design, the voltage-biased topology was instead chosen with a programmable resistor to control the amplitude. Compared to a standard current source, the programmable resistor has the advantage of being flicker noise free. Excessive Q-degradation was avoided by limiting the VCO amplitude.

The VCO resonator consists of:

- *5-bit DiCAD*: DiCAD is used to provide fine digital tuning. The differential series inductance of the transmission line is calculated as 34 pH, while the differential capacitance (when closed) of each of the 31 strips is approximately 3 fF. Since DiCAD is a distributed structure, the unit capacitor-cells, although identical, do not have the same effect on the oscillation frequency. Therefore, to ensure monotonicity, a thermometer code is used to digitally control the DiCAD.
- *Varactor*: To maximize the varactor tuning range for a given size and to eliminate variation with the core bias point, the varactor is typically AC-biased through large capacitors to the resonator. To save area and eliminate top/bottom plate capacitance, we coupled the varactor

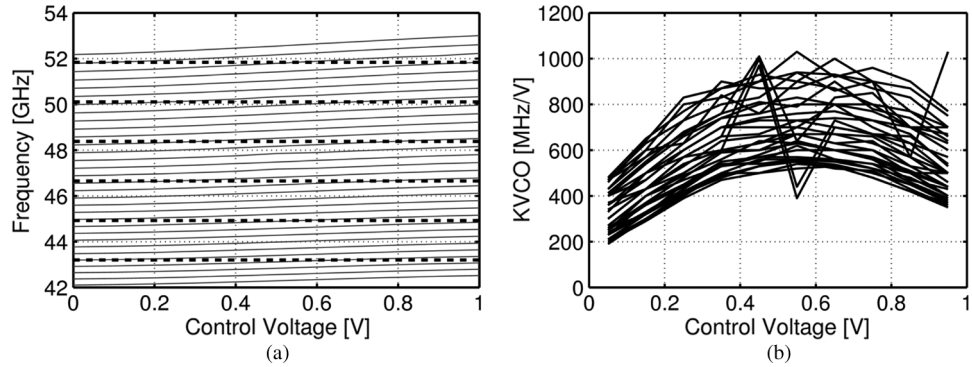


Fig. 9. Measurement of the VCO's continuous tuning characteristics. (a) The continuous tuning curves. (Heavy dotted lines correspond to frequencies that can be synthesized.) (b) $\mathrm{K_{VCO}}$ overlaid for all 32 DiCAD states. Discontinuities are due to measurement error.

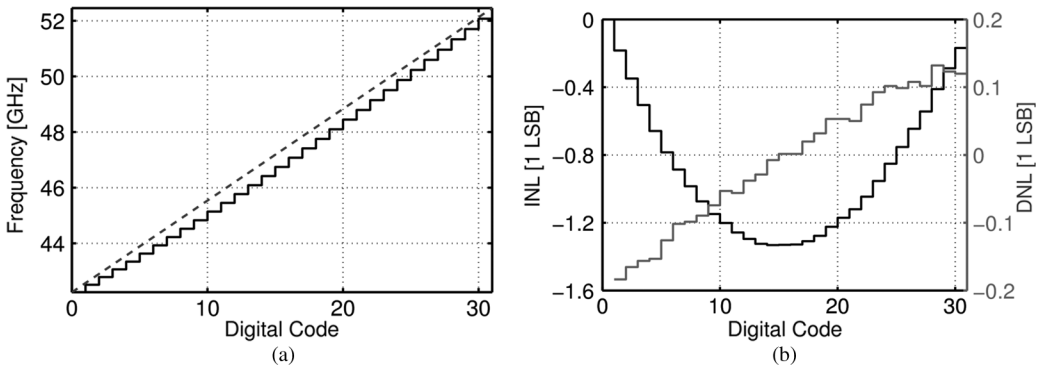


Fig. 10. Measurement of the VCO's discrete tuning characteristic. (a) The VCO oscillation frequency versus digital code (with $\mathrm{V_{CTRL}} = 0.5$ V). (b) The INL/DNL of VCO discrete tuning curves (with $\mathrm{V_{CTRL}} = 0.5$ V).

to the resonator through a transformer (XFMR). This is possible because of the large XFMR coupling coefficient observed at mm-wave ($>$0.8). The effective small-signal capacitance of the varactor ranges from 3 fF to 9 fF.

- *Single Turn Transformer*: The XFMR used to couple the varactor to the VCO core also contributes an effective 84 pH of inductance. The primary coil consists of a single turn inductor drawn on metal 6, while the secondary coil is an identically dimensioned and positioned inductor drawn on metal 5.

2) DiCAD-Based Injection-Locked Buffer and Divider: Since the PLL is intended for use in a TRX, a buffer is required to isolate the VCO from the signal path. To keep power consumption low, an injection-locked oscillator is employed as the buffer (Fig. 4). To ensure good frequency alignment, the injection-locked buffer has a very similar design approach and layout style to that of the oscillator. To account for the different load capacitance, there are, however, differences: the main inductance is smaller, while the DiCAD switches are also reduced in size to maintain the required frequency range (we are less concerned with resonator-Q in the buffer as it does not impact phase noise.)

The first divide-by-2 stage is also an injection-locked topology [19] (Fig. 4). Although the divider could be realized by an aggressive CML design, the injection-locked topology is a low power option. As in the design of the buffer, precise frequency alignment is needed to ensure that the PLL lock over the entire VCO tuning range. This requires that the free running frequency of divider is close to half that of the VCO/Buffer. Accordingly, DiCAD is employed in both blocks to tune the resonators to the appropriate frequency. As in the VCO, 5-bit DiCAD is used in the buffer. The divider locking range is wide enough that only 4-bit DiCAD is required. Naturally, when employed in a full system, the DiCAD states of the VCO, buffer and divider need to be calibrated on chip. Provided locking time is not critical, this calibration can be accomplished using the straightforward scheme presented in Section V.

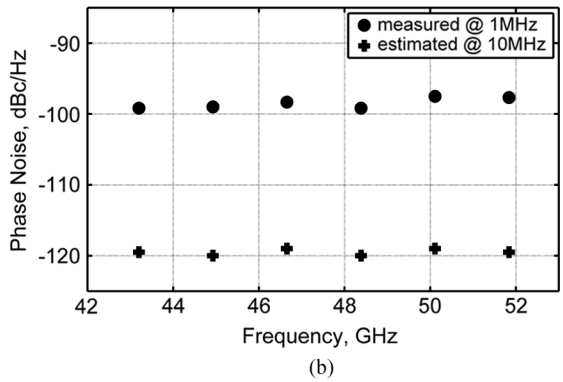
V. Measurement Results

The PLL, shown in Fig. 3, was fabricated in a 65 nm GP process. An on-chip Serial-to-Parallel Interface (SPI) controls 48 bit-lines that are used for digital control current, digital frequency tuning and other various control lines. A PTAT current reference is used to provide accurate bias currents. The 48 GHz injection-locked buffer drives two open drain buffers that are probed directly using GSSG probes. The control voltage is connected directly to a pad so that VCO tuning curves can be measured and the loop bandwidth can be modified during testing. The reference is provided by an ultra-low-noise 54 MHz Crystek XO.

The measured VCO tuning curves are shown in Fig. 9. Continuous tuning from 42.1 GHz to 53 GHz is achieved with a $\mathrm{K_{VCO}}$ of less than 1 GHz/V. The worst case band overlap is approximately 50%. Fig. 10 plots the VCO frequency versus

Freq. [GHz]	Phase Noise [dBc/Hz]	FOM [dBc/Hz]	FOM_T [dBc/Hz]
43.2	-99.17	-179.84	-187.04
44.928	-99	-180.01	-187.21
46.656	-99.33	-179.67	-186.87
48.384	-99.17	-180.82	-188.02
50.112	-97.5	-179.46	-186.66
51.84	-97.67	-179.92	-187.12

(a)



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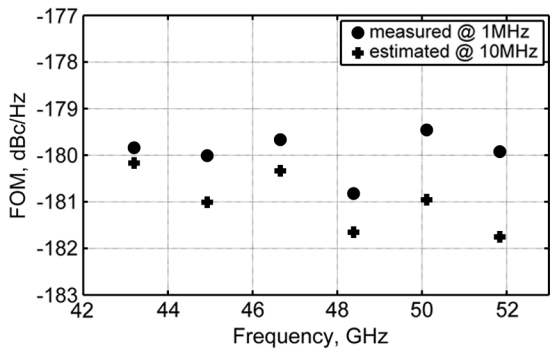

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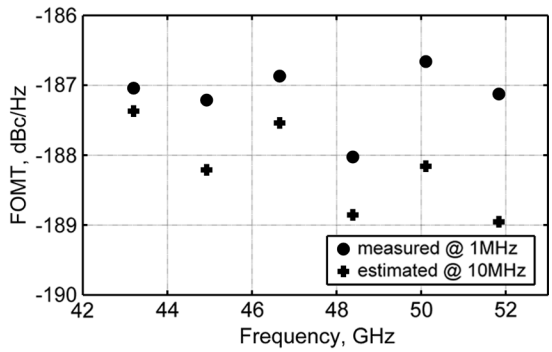
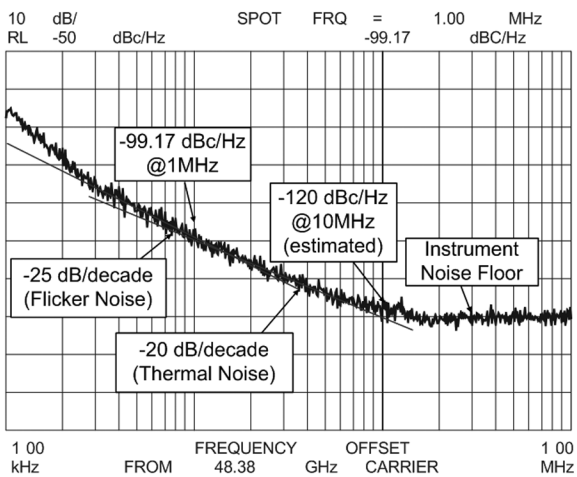
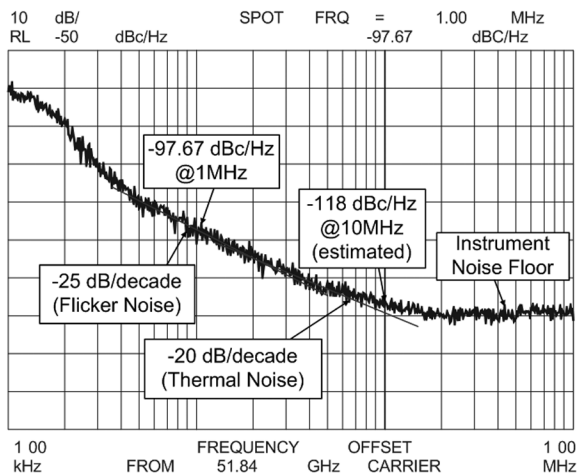


(d)

Fig. 11. The performance metrics of the DiCAD-VCO across entire frequency band. (a) Table of performance metrics. (b) Phase noise measurements. (c) Figure of merit. (d) Figure of merit including tuning range.



(a)



(b)

Fig. 12. The closed loop phase noise measurements with a large off-chip loop filter. (a) Phase noise @ 48.384 GHz. (b) Phase noise @ 51.84 GHz.

the DiCAD state and clearly shows the distributed nature of DiCAD; a conventional switched capacitor bank would result in non-uniform frequency steps that widen at higher frequencies, by contrast, DiCAD tuning results in very fine, monotonic digital tuning that is remarkably linear, as shown in the digital INL/DNL plots of Fig. 10(b). This is due solely to the distributed nature of DiCAD, since the effective capacitance of identical DiCAD strips (as observed from the differential pair) reduces as you move along the DiCAD structure. Because of this, a thermometer code is used where the LSB is closest to the XFMR and the MSB is closest to the differential pair; reversing the direction would result in a frequency spacing that is even more non-uniform than would be expected using a lumped switched capacitor-bank.

Under closed-loop operation, the PLL is capable of generating six equally spaced tones: 43.2 GHz, 44.928 GHz, 46.656 GHz, 48.384 GHz, 50.112 GHz, and 51.84 GHz. The latter four tones are precisely 4/5 of the channel frequencies defined in the IEEE 802.15.3c standard and are suitable for a heterodyne IEEE 802.15.3c TRX with $\mathrm{F_{TRX}} = (5/4) \times \mathrm{F_{LO}} = 5 \times \mathrm{F_{IF}}$. The achievable out-of-band noise (i.e., noise which appears outside the loop bandwidth

TABLE I
COMPARISON WITH REPORTED CMOS mm-WAVE VCOS

Reference	[13] JSSC '07	[20] VLSI-DAT '09	[21] JSSC '09	[17] RFIC '10	This Work
Technology	0.18µm CMOS	0.18µm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Centre Frequency [GHz]	40	47.9	58.4	39.9	47.55
Supply [V]	1.5	1.2	0.7	1.2	1
Phase Noise @ 1MHz [dBc/Hz]	-100.2	-102.5	-91	-98.1	-97.5
Power [mW]	27	5.6	8.1	14.4	16
Core Area [μm^2]	900 x 200[§]	N/A	96 x 80	300 x 500	220 x 125
Tuning Range [%]	20	1.59	9.32	15.1	22.9
FOM_T [dBc/Hz] [‡]	-183.9	-172.7	-176.6	-182.1	-186.66

[§]Estimated from dimension of complete chip
[‡]$FOM_T = PN\{\Delta\omega\} + 20\log10(\omega_0/\Delta\omega) - 10\log10(PDC[mW]) + 20\log10(TR/10)$

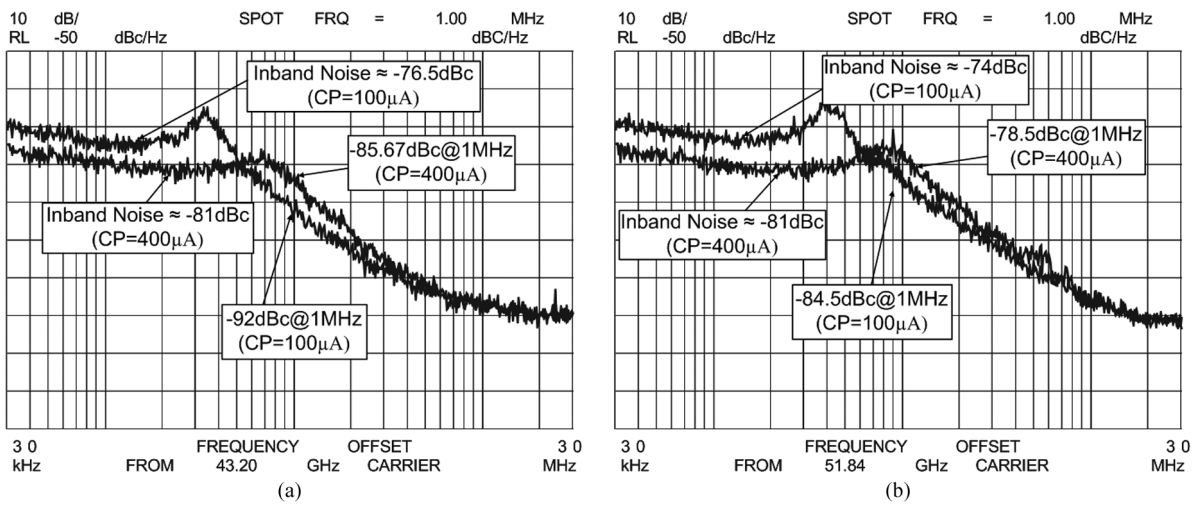


Fig. 13. The closed loop phase noise measurements with on-chip loop filter enabled. (a) Phase noise @ 43.20 GHz. (b) Phase noise @ 51.84 GHz.

of the PLL) is measured using a large off-chip loop filter that reduces the PLL loop bandwidth to less than 100 kHz. Phase noise measurements and other performance metrics are listed in Fig. 11, and typical outputs from the spectrum analyzer are shown in Fig. 12. Note that the noise performance is maintained across the entire band. This fact is important, as a wideband PLL that employs a large varactor to cover the entire tuning range will experience a flicker-noise null at a single point [9]. Since the out-of-band noise is basically the noise contribution of the VCO itself, Table I compares the DiCAD-VCO with recently reported mm-wave CMOS VCOs. When performance across the entire band is considered, the DiCAD-VCO achieves the best performance in terms of tuning range and oscillator figure of merit, $\mathrm{FOM_T}$.

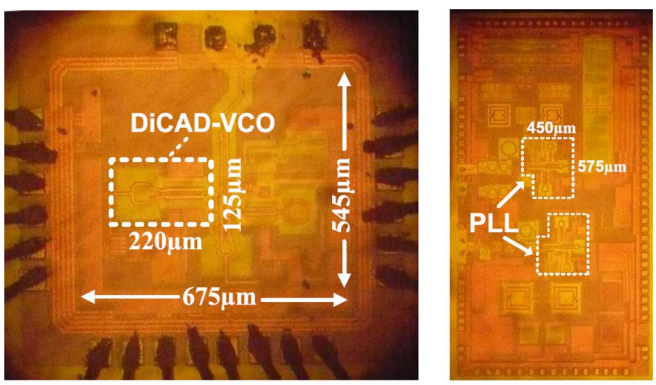
Ultimately, the transceiver's BER is limited by RMS jitter, which depends on both VCO noise and the inband noise [22]. When the on-chip loop filter is enabled, the loop bandwidth sits around 1 MHz and the inband noise is measured at -81 dBc/Hz (Fig. 13). This number is as good as or better than other standard integer-N topologies that employ similar divide ratios [4], [18], and can be reduced further by increasing the charge pump current (although charge pump noise dominates the inband noise profile of this design, only 400 μA is currently dissipated in the charge pump, which is relatively small compared to the total power consumption of the chip). The I/Q signals were not brought off-chip and could not be measured.

Table II compares our PLL design with recent publications. Compared to the state-of-the-art [6], our work improves normalized phase noise, covers an additional 60 GHz band, consumes less power and 64% less area, and operates at a higher frequency. More importantly, the VCO also directly generates the $\mathrm{F_{LO}}$ frequency. This is in contrast to [6], which isolates the second harmonic of a push-push QVCO operating at $\mathrm{F_{LO}}/2$. Therefore, we avoid the problem of limited second harmonic drive strength and all issues associated with QVCOs (unpredictable mode behaviour, increased I/Q mismatch, increased area). The die micrograph of the testchip is shown in Fig. 14(a). The PLL is intended for use in a dual-synthesizer TRX and a micrograph of that chip is shown in Fig. 14(b).

TABLE II
COMPARISON OF PLL WITH STATE OF THE ART

Reference	[4] ESSCIRC '07	[5] ISSCC '09	[6] ISSCC '10	This Work
Technology	90nm CMOS	45nm LP CMOS	65nm LP CMOS	65nm GP CMOS
Architecture	Integer-N (VCO @ 60GHz)	Integer-N (QVCO @ 60GHz)	Integer-N (QVCO @ 20.88GHz)	Integer-N (VCO @ 50.112 GHz)
Frequency Range	61.1-63.1	57-66	35-41.88	42.1-53
Supply[V]	1.2	1.1	1.2§	1
Phase Noise (normalised to Band 3) [dBc/Hz @ 1MHz]	-80	-75	-90.46‡ -93.98⊤	-95.56†
Reference Frequency [MHz]	60	100	36	54
Power [mW]	78	78	80	72
IEEE 802.15.3c Band Coverage	1 Band	All 4 Bands	3 Bands	All 4 Bands
Core Area [μm^2]	600 x 600	N/A	1100 x 1000	680 x 550
VCO Tuning Range [%]	3.2	14.6	17.9	22.9
Inband Phase Noise[dBc/Hz]	-72	-75	N/A	-81

§1.8 V used for CP/PFD.
†Normalized to 62.64 GHz (Band 3) from 50.112 Hz measurement.
‡Normalized to 62.64 GHz (Band 3) from 20.88 Hz measurement.
⊤ Normalized to 62.64 GHz (Band 3) from 41.96 Hz measurement.



(a) (b)

Fig. 14. The chip micrographs. (a) PLL testchip with DiCAD-VCO highlighted. (b) Dual PLL TRX testchip.

As with any PLL, the free-running frequency of the VCO must be close to the desired synthesized frequency to allow the control voltage to lock the PLL. In this design, the same is true for the mm-wave buffer and 24 GHz divider, which are also capable of operating as free-running oscillators. This means the DiCAD states in the VCO, buffer and divider must be appropriately chosen in order for the PLL to successfully lock.[4] A method to calibrate injection locked dividers within the PLL has already been demonstrated [23]. In our 60 GHz solution, we are less concerned with locking time and, therefore, intend to use a far simpler closed-loop calibration scheme. Firstly, we assume that the VCO and buffer frequencies are closely aligned and are always set to the same bit. Then, using the algorithm outlined in Fig. 15(a), we sweep the VCO/Buffer and divider control bits while monitoring the control voltage. Once the control voltage settles to value that is not ground or the power rail, the PLL can be considered locked. To replicate a complete TRX SOC, the control voltage is digitized using an off-chip ADC. The algorithm (which can be run in a microcontroller) monitors the digitized control voltage and changes the frequency settings using the on-chip SPI. Four chips were tested and all of them successfully locked across all four bands. Examples of the locking algorithm are shown in Fig. 15(b) and (c). More sophisticated schemes, such as [23], can be employed if a faster locking time is required.

[4]The measurements presented thus far were obtained by manually tuning the digital control bits of the VCO, buffer and divider. These results demonstrate the performance capability (e.g., tuning range, phase noise, etc.) of the PLL provided it has been appropriately calibrated.

VI. CONCLUSION

A low-noise, wideband PLL that can support a complete IEEE 802.15.3c TRX is reported. The circuit is simple and robust, and the LO tone is generated by the fundamental of the VCO rather than by some harmonic. Further, by embedding a tunable transmission line in all mm-wave blocks, the synthesizer achieves state-of-art performance (i.e., phase noise, area,

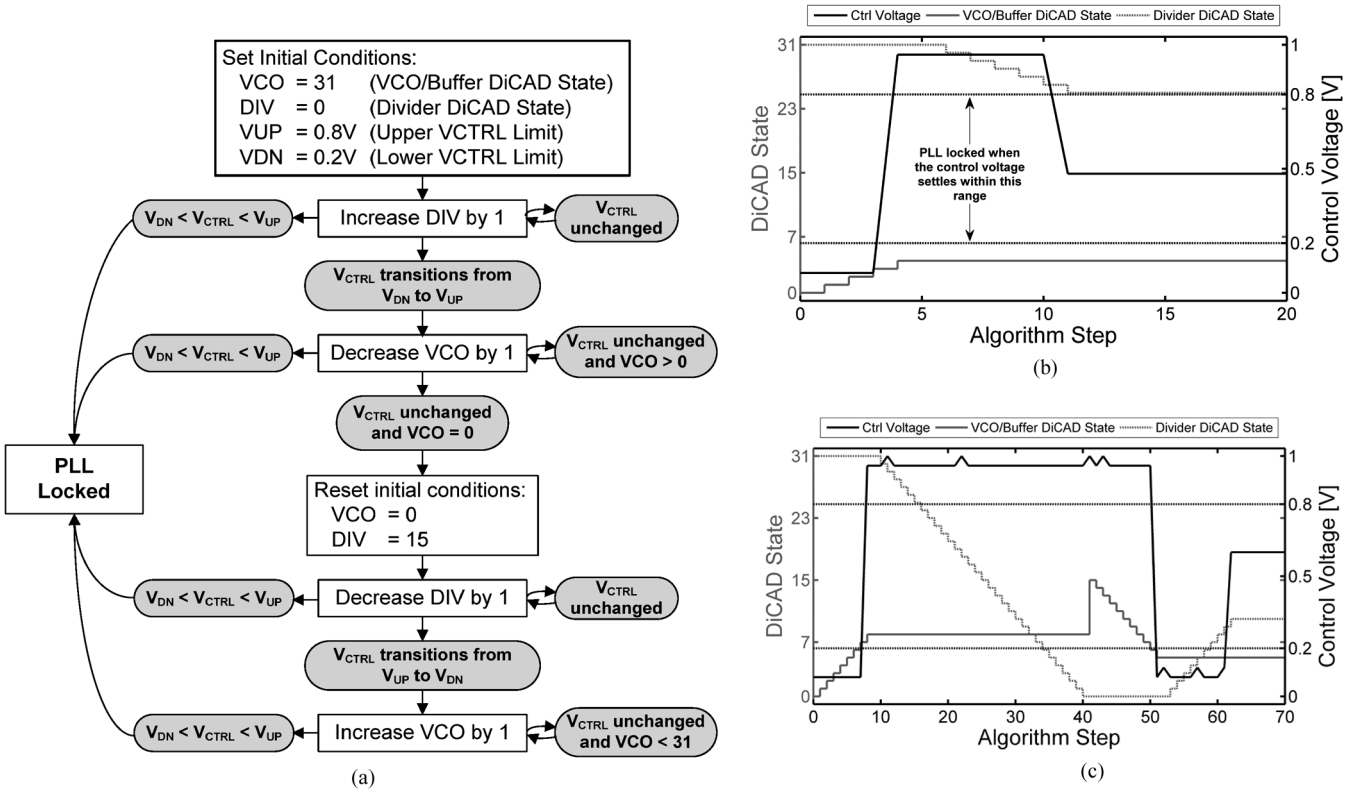


Fig. 15. The calibration algorithm used to align the centre frequencies of the VCO, buffer and first stage divider. (a) Algorithm Outline; VCO/Buffer and divider DiCAD states are swept until the control voltage settles within the 0.2 V–0.8 V range. (b) Calibration of testchip 1 locking to 50.112 GHz. (c) Calibration of testchip 2 locking to 44.928 GHz.

frequency coverage, power) that is maintained across the entire band.

ACKNOWLEDGMENT

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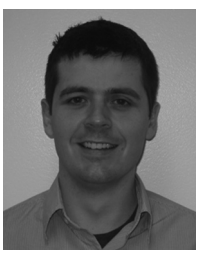

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(Planar HBT/MESFET) integrated circuit technologies from the research laboratory to the production line (now Conexant Systems and Skyworks). The HBT/BiFET productions have grown into multi-billion dollar businesses and dominated the cell phone power amplifiers and front-end module markets (currently exceeding one billion units/year). Throughout his career, his research has primarily focused on the development of high-speed semiconductor devices and integrated circuits for RF and mixed-signal communication and imaging system applications. He was the principal investigator at Rockwell in leading DARPA's ultra-high speed ADC/DAC development for direct conversion transceiver (DCT) and digital radar receivers (DRR) systems. He was the inventor of the multiband, reconfigurable RF-Interconnects, based on FDMA and CDMA multiple access algorithms, for ChipMulti-Processor (CMP) inter-core communications and inter-chip CPU-to-Memory communications. He also pioneered the development of world's first multi-gigabit/sec ADC, DAC and DDS in both GaAs HBTs and Si CMOS technologies; the first 60 GHz radio transceiver front-end based on transformer-folded-cascode (Origami) high-linearity circuit topology; and the low phase noise CMOS VCO (FOM <-200 dBc/Hz) with Digitally Controlled on-chip Artificial Dielectric (DiCAD). He was also the first to demonstrate CMOS oscillators in the Terahertz frequency spectrum (1.3 THz) and the first to demonstrate a CMOS active imager at the sub-millimeter-wave spectra based on a Time-Encoded Digital Regenerative Receiver. He was also the founder of an RF design company G-Plus (now SST Communications) to commercialize WiFi 11b/g/a/n power amplifiers, front-end modules and CMOS transceivers.

Prof. Chang was elected to the U.S. National Academy of Engineering in 2008 for the development and commercialization of GaAs power amplifiers and integrated circuits. He was also elected as a Fellow of IEEE in 1996 and received the IEEE David Sarnoff Award in 2006 for developing and commercializing HBT power amplifiers for modern wireless communication systems. He was the recipient of the 2008 Pan Wen Yuan Foundation Award and 2009 CE-SASC Career Achievement Award for his fundamental contributions in developing AlGaAs/GaAs heterojunction bipolar transistors. His recent paper "CMP Network-on-Chip Overlaid with Multiband RF-Interconnect" was selected for the Best Paper Award at the 2008 IEEE International Symposium on High-Performance Computer Architecture (HPCA). He received Rockwell's Leonardo Da Vinci Award (Engineer of the Year) in 1992; National Chiao Tung University's Distinguished Alumnus Award in 1997; and National Tsing Hua University's Distinguished Engineering Alumnus Award in 2002.