CMOS Prescaler(s) With Maximum 208-GHz Dividing Speed and 37-GHz Time-Interleaved Dual-Injection Locking Range

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***Abstract*—To enable CMOS prescaler(s) for submillimeter-wave radio-frequency synthesis, we present a new dynamic frequency divider topology according to a time-interleaved dual-injection locking scheme. Consequently, the prototype prescalers implemented with 65-nm CMOS technology have demonstrated ultrahigh operation speeds up to 208 GHz, with ultrawide locking range up to 37 GHz, with 2.5-mW power consumption. The achieved performance figure of merit (FOM) [i.e., (speed $\times$ range)/power in GHz^2/mW] is roughly an order of magnitude higher than that of the state of the art.**

***Index Terms*—CMOS prescaler, injection locking frequency divider, submillimeter wave circuits, wide locking range.**

I. Introduction

ELECTROMAGNETIC wave spectra beyond that of the millimeter-wave frequencies have attracted increasing interests for facilitating multigigabit/second wireless communications and through-fabric/fog imaging systems [1]. CMOS starts to play roles in such applications due to its substantially increased device speed driven by the continuous technology scaling. For example, the f_T and $f_{\max}$ of 65-nm CMOS are beyond 200 GHz and make it feasible for emerging millimeter-/submillimeter-wave system applications. In conjunction with the voltage-controlled oscillator (VCO), the prescaler is one of the most challenging circuit building blocks due to the stringent system requirements on high dividing frequency, wide locking range, excellent input sensitivity, and low power consumption. For achieving the aforementioned design objectives, we have demonstrated a G-band prescaler for the first time in 65-nm CMOS with a unique time-interleaved dual-injection locking scheme for extended locking range and reduced power consumption.

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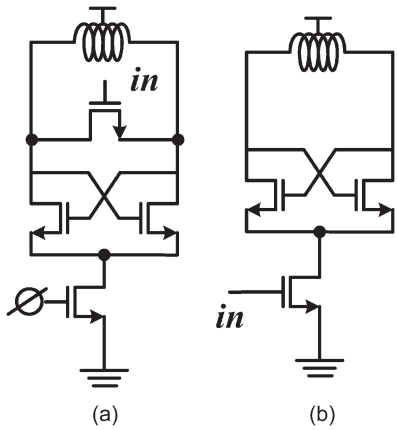

Fig. 1. Two widely used high-frequency divider schemes.

II. Submillimeter-Wave Prescaler Design Challenges

Although shorter-channel CMOS devices offer higher operation frequency, there still exits serious dilemmas between the high dividing frequency and the wide locking range in submillimeter-wave frequency divider design. Higher dividing frequency generally demands smaller L and C with higher tank Q to achieve sufficient oscillation gain. Nonetheless, the higher tank Q often leads to narrower locking range [2]. Such tradeoff becomes more prominent when the dividing frequency is higher. For example, [3] demonstrated a 14% locking arrange with lower than 100-GHz dividing frequency, whereas [4] and [5] achieved higher dividing frequencies of 120 and 130 GHz, respectively, with a much smaller locking range of 7%. Therefore, a new frequency divider scheme is desired to attain both high dividing frequency and wide locking range for millimeter- and/or submillimeter-wave frequencies.

Two typical types of high-speed frequency dividers are depicted in Fig. 1(a) and (b), respectively. In the first type [see Fig. 1(a)], the input or injection device shunts between the cross-connect differential pair outputs, which not only increases the tank loading but also limits the injection efficiency. To improve the injection efficiency, [3] had adopted complimentary n/p-channel devices in parallel, which, however, decreased the maximum operation frequency due to an extra p-channel device parasitic. In the second type [see Fig. 1(b)], the common source node might shunt a substantial portion of the input signal current to ground via a large capacitive parasitic of the node

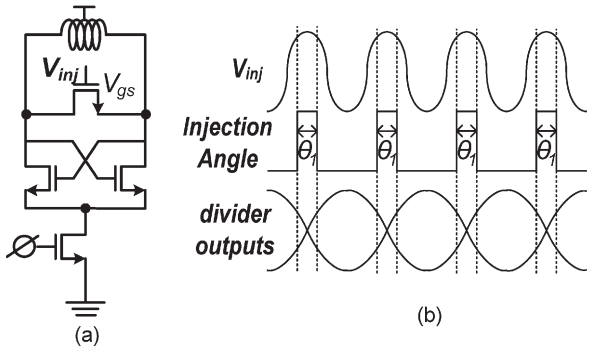

Fig. 2. (a) Typical voltage-injection scheme. (b) The most effective injection angle θ_1 occurs around divider output crossing points.

and consequently degraded the injection efficiency. Wu and Hajimiri [6] utilized an additional inductor to resonate out the parasitic capacitance for obtaining higher injection efficiency. However, the added resonant tank greatly limited the locking range and consumed extra chip area.

III. Voltage and Current Injection

Although the two existing injection schemes have their own shortcomings to achieve simultaneously high dividing frequency and wide locking range, they each has certain unique features that can be selectively adopted to constitute a better prescaler scheme.

For instance, the first type [see Fig. 2(a)] injects a voltage signal into an NMOS mixing device that shunts between the cross-couple pair outputs. As the injection voltage (Vgs) exceeds the device threshold, the device turns on and introduces a low impedance path to pull its source/drain (or the cross-couple pair outputs) voltages closer. This thus generates a pulling force to bring divider outputs toward the crossing points [see Fig. 2(b)], whereas the injections deviate from the output crossings. Provided that the divider's natural oscillation frequency is close to one half of the injection frequency, this effect will eventually align the divider output frequency and phase with that of the voltage injection. Consequently, output crossing times will be synchronized with the effective voltage injection region of angle θ_1.

The second type injects current signals through a common current source device [see Fig. 3(a)]. Around the output crossing point, the currents are equally distributed via differential branches to result in a common mode with negligible injection effect. On the contrary, the highest injection efficiency occurs near the output peak, where the injection current feeds through only one of the two branches. This can be further comprehended by assuming the following: 1) The injection frequency is at twice of the autonomous oscillation frequency; 2) the oscillator output voltages are $\pm V_o \cos(\varpi_o t)$; 3) the injection current at the common source node is $I\cos(2\varpi_o t + \phi)$; and 4) the current is steered to the left side by gate voltage $V_o \cos(\varpi_o t)$ and mixes with it to generate the drain voltage, i.e.,

$$\begin{aligned} V_d &= -V_o \cos(\varpi_o t) \times I\cos(2\varpi_o t + \phi) \times R_p \\ &= -V_o I R_p \left[\cos(\varpi_o t + \phi) + \cos(3\varpi_o t + \phi)\right]/2 \end{aligned} \quad (1)$$

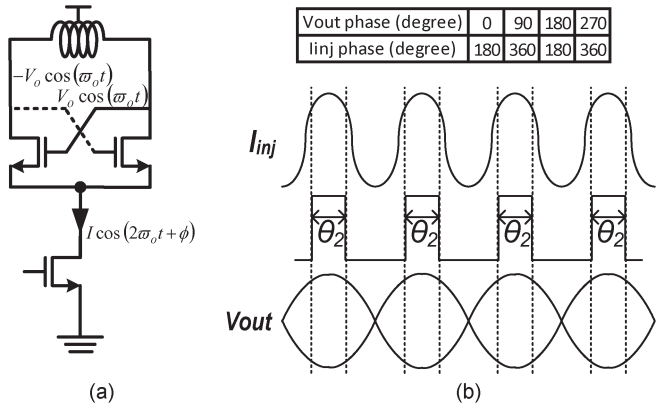

Fig. 3. (a) Current injection scheme. (b) The most effective injection angle θ_2 occurs around output peak points.

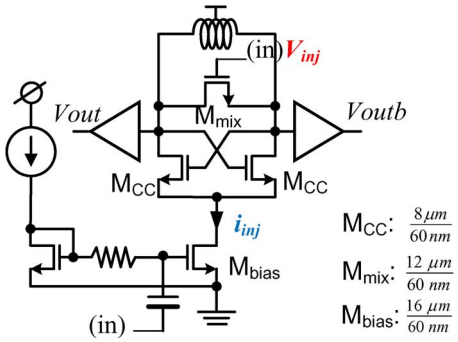

Fig. 4. Prescaler topology based on the proposed time-interleaved injection locking scheme to boost locking range.

where R_P is the equivalent tank parallel impedance. Given the natural tank filtering, only the first item with ϖ_o would survive and equal to $-V_o\cos(\varpi_o t)$ with $\phi = 180$ mandated by the cross-couple pair. The phase relationship between the injection current and output voltage is then tabulated and drawn in Fig. 3(b). It aligns the maximum current injections with the peak output voltages. Consequently, as the divider's natural oscillation frequency approaches to half of the injection frequency, the current injection will synchronize the frequency and phase of divider outputs with the current injections of θ_2 as an effective injection angle.

IV. Proposed Prescaler

A. Proposed Prescaler Architecture and Working Mechanism

Since the effective injection angles for two different divider types are time interleaved, they can join force to structure the prescaler with an unprecedented dual-injection locking. As illustrated in Fig. 4, the input signal is injected to both the top voltage mixing device and the bottom current source device to attain extended injection angle that can lead to simultaneously higher autonomous oscillation frequency and wider locking range. The detailed dual-injection locking mechanism can be further analyzed based on a physical circuit modeling given as follows.

Since the effective voltage injection angle θ_1 is roughly centered at the crossing point of divider output, as shown in

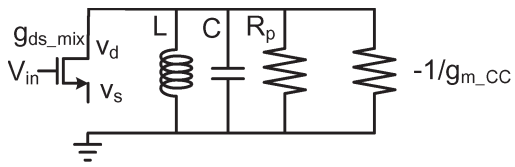

Fig. 5. Small signal model during voltage injection.

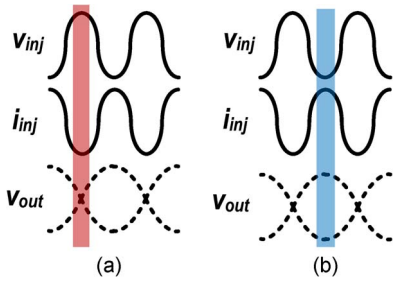

Fig. 6. (a) Injection current is at minimum during voltage injection. (b) Injection voltage is at minimum during current injection.

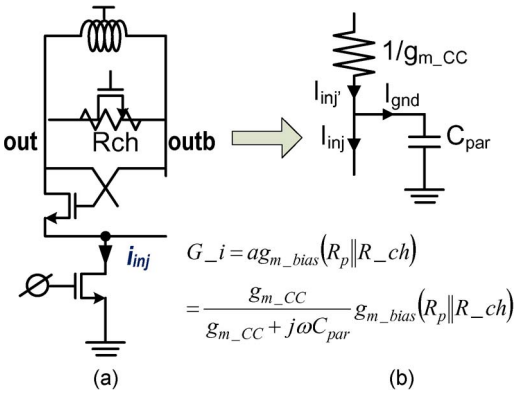

Fig. 7. (a) Current injection equivalent circuit and (b) common source node current division due to parasitic capacitance, which degrades overall gain.

Fig. 2(b), we can derive the small signal gain of the voltage mixing device from the source to drain as (2) based on a simplified small signal model as shown in Fig. 5, i.e.,

$$G\_v = \frac{V_d}{V_s} = g_{ds\_\mathrm{mix}} \times R_{\mathrm{load}} = g_{ds\_\mathrm{mix}} \times (R_P /\!\!/ -1/g_{m\_\mathrm{cc}}) \tag{2}$$

where g_{ds_mix} is the transconductance of the input mixing device at the triode region and $g_{m\_\mathrm{cc}} = \sqrt{\mu_n \times C_{\mathrm{ox}} \times I \times w/l}$ is the transconductance of the cross-couple device around the crossing point. The small signal gain in (2) must exceed the unity, and the overall impedance must be kept positive during the injection period to ensure the locking operation, i.e., $g_{m\_\mathrm{cc}} < (1/R_P)$, and to suppress the frequency divider from oscillating at its autonomous frequency. Thus, g_{m_cc} at crossing points needs to be reduced, which coincides with the case that I is the smallest at crossing couple points, as shown in Fig. 6(a).

On the other hand, the current injection happens around the output voltage peak points, as shown in Fig. 7(a). The small signal gain is

$$G\_i = \alpha \times g_{m\_\mathrm{bias}} \times R_p /\!\!/ R_{\mathrm{ch\_mix}} \tag{3}$$

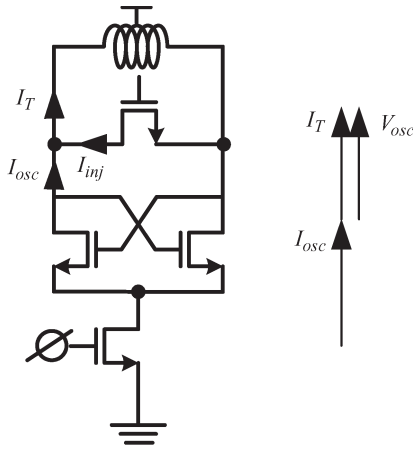

Fig. 8. Phase relationship with no injection.

where α refers to the injection ratio, which is determined by the current division due to parasitic capacitance at the common source node, i.e., $\alpha = g_{m\_\mathrm{cc}}/(g_{m\_\mathrm{cc}} + j\varpi C_{\mathrm{par}})$, based on Fig. 7(b). g_{m_bias} is the transconductance of the bottom current source device, and $R_{\mathrm{ch\_mix}}$ is the channel resistance of the voltage injection input mixing device. To maximize the injection gain, large load impedance is desired, which can be met when $R_{\mathrm{ch\_mix}}$ reaches the maximum with the switching device off. As shown in Fig. 6(b), it again matches with the injection cycle of the prescaler, where the input voltage is minimum during the output peak periods and turns off the device to reduce the tank loading.

B. Locking Range Analysis

When there is no injection signal, the prescaler behaves as an oscillator with its own autonomous resonant frequency. As shown in Fig. 8, tank current I_T, oscillator current I_{osc}, and output voltage V_{out} are in-phase. When input frequency is exactly twice of the oscillator autonomous frequency, injection current I_{inj} is also in-phase with tank current I_T and oscillator current I_{osc}, where the input voltage aligns with the output crossing point. When input frequency is lower than twice of the oscillator autonomous frequency, I_T lags behind I_{osc} by phase θ, which requires I_{inj} compensating the phase difference. Additionally, the input voltage is later than the output crossing point shown in Fig. 9(a). Vice verse, when input frequency is higher than twice of the oscillator autonomous frequency, I_T leads I_{osc}, and the input voltage is earlier than the output crossing point shown in Fig. 9(b). Similar analysis can be derived in the current injection scheme that input frequency determines the phase relationship between input current and output voltage as well.

The phase compensation requirements for different frequencies, demonstrated in Fig. 9, leads to the prescaler locking range constraints, which is specified in (4) with detailed derivation from [7] and [8], i.e.,

$$\Delta\omega \approx \frac{\omega_o}{2Q}\frac{I_{\mathrm{inj}}}{I_{\mathrm{osc}}}. \tag{4}$$

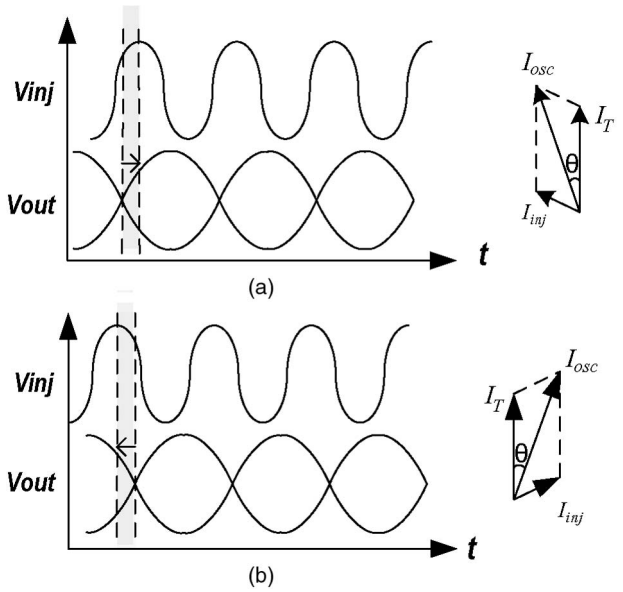

Fig. 9. Phase relationship between injection, oscillation, and tank currents at different input frequencies. (a) Input frequency $<$ twice of autonomous oscillation frequency. (b) Input frequency $>$ twice of autonomous oscillation frequency.

In the case of current injection, the heavy loaded common source node shunts a large portion of injection current to the ground, which dramatically degrades the injection efficiency through factor α, as discussed in Section IV. The higher the frequency, the smaller α, and the poorer injection efficiency is. That is the reason why this structure alone has resulted in very narrow locking range in high operation frequency cases.

With this novel dual-injection locking scheme, the overall injection strength is boosted by two means. First is the added injection strength due to both voltage and current injection. Second, and more important, the interleaving injection renders smaller current during voltage injection period that is equivalent to lower oscillator current $I_{\rm osc}$ and thus increases the $I_{\rm inj}/I_{\rm osc}$ ratio for extended locking range. Using factor γ to stand for the phase relationship between the voltage injection and current injection, the time-interleaving locking range can be elaborated from (4) as

$$\Delta\omega \approx \frac{\omega_o}{2Q}\left(\frac{I_{\rm inj\_}v}{\gamma \times I_{\rm osc}} + \frac{\alpha \times I_{\rm inj\_}i}{I_{\rm osc}}\right) \tag{5}$$

as γ reaches its minimum when voltage and current injections are 180° out of phase to provide the prescaler with the maximum locking range. When the phase difference deviates from 180°, factor γ gets larger and injection efficiency decreases. Fig. 10 shows the simulated locking range versus the phase difference Θ between the voltage and current injections. It validates the locking range maximizing at $\Theta = 180$ degree and gradually decreasing as Θ deviates from 180°.

Fortunately, 180° phase difference is natural for CMOS VCO to provide fully differential injection signals. However, it is quite challenging to generate truly differential signals at 200 GHz for this standalone prescaler testing. Instead, we have implemented a single-ended test chip. With the delays of the transmission line and the gate voltage to drain current from the current source device, the phase difference Θ is only about 90° in this prototype.

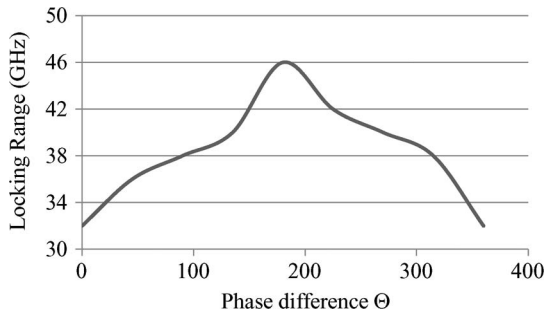

Fig. 10. Simulated prescaler locking range versus phase relationship between voltage and current injection.

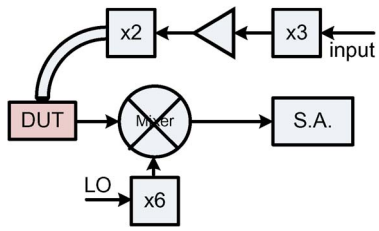

Fig. 11. Measurement setup.

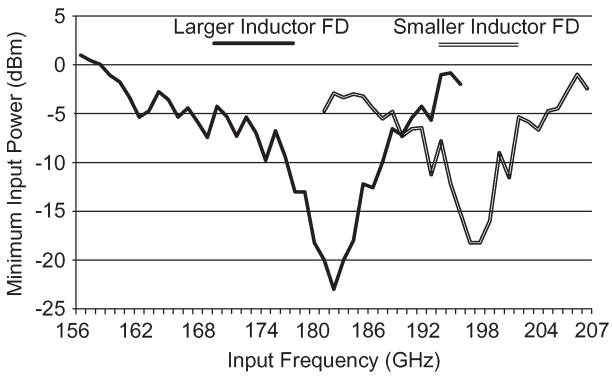

Fig. 12. Measured input sensitivities for the two prescalers.

V. Measurement Results

Fig. 11 shows the measurement setup. The signal from an external frequency synthesizer drives cascaded multiply-by-3, PA and multiply-by-2 circuits to produce the desired G-band input signal for the testing. After device under test, the G-band signal is divided and the output is down-converted by an external mixer to feed into a spectrum analyzer to acquire the divided signal output [9].

Two prescalers with different inductor values (about 120 and 150 pH, respectively) are implemented, with simulated inductor quality factors about 20. The measured input sensitivities of both prescalers are elucidated by drawing the minimum input power versus the input frequency, as shown in Fig. 12. The demonstrated locking ranges are over 37 GHz (158–195 GHz or 21%) with $<$ 0 dBm input power and 27 GHz (181–208 GHz or 14%) with < -1 dBm input power, respectively.

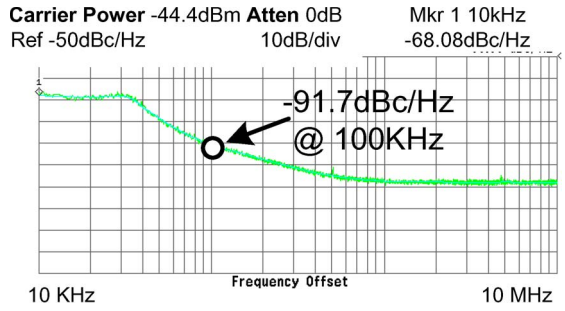

Fig. 13. Measured prescaler output phase noise.

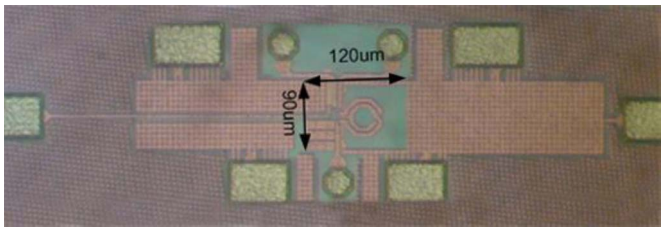

Fig. 14. Die photo of CMOS prescaler with time-interleaved dual injection locking scheme.

TABLE I
PERFORMANCE COMPARISON WITH CMOS STATE OF THE ART

	[3]	[4]	[5]	This Work	
Technology	65nm	90nm	65nm	65nm	65nm
Center Frequency	89GHz	121GHz	200GHz	176.5GHz	194.5GHz
Locking Range	82~94GHz (12GHz)	117~125GHz (8GHz)	199~201GHz (2GHz)	158~195GHz (37GHz)	181~208GHz (27GHz)
Input Power	0 dBm	N/A	<-15dBm	0dBm	-1dBm
Phase Noise	N/A	N/A	N/A	-91.7dBc/Hz @100KHz	-91.6dBc/Hz @100KHz
Power Consumption	3.92 mW	10.5 mW	8.8 mW	2.4mW	2.4mW
Chip Area	N/A	0.3mmX 0.14mm	0.2mmX 0.16mm	0.12mmX 0.09mm	0.12mmX 0.09mm
FOM (GHzXGHz/mW)	272	92	45^{Δ}	2721	2188

$^{\Delta}$: only lower input power results available

Fig. 13 presents one prescaler output phase noise (PN), about -91.6 dBc/Hz at 100-kHz offset. The other prescaler shows similar PN performance. The PN is limited by the external local oscillator, which is 1/6 of the output frequency with PN measured of -107 dBc/Hz at 100 kHz. Therefore, output PN will have degradation of $20 \times \log(6) = 15.6$ dB. Thus, prescalers' noise contribution is negligible. Both prescalers draw about 2.4 mA from a 1-V power supply. A chip photo is shown in Fig. 14 with the core chip area 0.12 mm $\times$ 0.09 mm. Both prescalers possess the same area with only different inductors.

Table I summarizes key performance measured from both prescalers and in comparison with the state of the art. It shows that their performance have substantially exceeded prior arts in terms of dividing frequency, locking range, and power consumption, which are the divider's key specifications. Therefore, we define an FOM to include all the key specs as

$$\text{FOM} = \text{Center Frequency} \times \text{Locking Range/Power}$$

where the center frequency and locking range are in gigahertz (i.e., GHz) and power consumption in milliwatt (i.e., mW). The measured FOMs of our two prescalers are 2721 and 2188 GHz^2/mW, respectively, which in either case are about ten times higher than that of prior arts.

VI. CONCLUSION

In summary, this paper has demonstrated a unique time-interleaved dual-injection locking scheme for CMOS prescalers to achieve the highest dividing frequency (195 GHz/208 GHz) ever reported for any semiconductor technology (versus SiGe [10] and InP heterojunction bipolar transistor [11]), simultaneously with wide locking range (37 GHz/27 GHz), high input sensitivity (< -1 dBm/0 dBm across the bands), low PN (< -91 dBc/Hz at 100 kHz offset), as well as low power consumption (2.4 mW). The combined FOM (2721/2188 GHz^2/mW) in either case has exceeded that of prior arts by almost ten times. The demonstrated time-interleaved dual injection prescalers have paved the road to implement high-precision frequency synthesizers in CMOS technology for integrated millimeter- and submillimeter-wave communication/imaging systems.

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