Sub-Millimeter Wave Signal Generation and Detection in CMOS

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***Abstract* — Feasibility of CMOS circuits operating at frequencies in the upper millimeter wave and low sub-millimeter frequency regions has been demonstrated. A 140-GHz fundamental mode VCO and a 324-GHz quadruple pushed VCO in 90-nm CMOS, a 410-GHz push-push VCO in 45-nm CMOS, and 180-GHz Schottky diode and 780-GHz plasma wave detectors in 130-nm CMOS have been demonstrated. With the continued scaling of MOS transistors, 1-THz CMOS circuits will be possible.**

***Index Terms* — CMOS, mm-wave, sub-millimeter wave, oscillator, Schottky diode, detector, phase locked loop, terahertz.**

I. Introduction

Electro-magnetic waves in the sub-millimeter wave frequency range (0.3-3THz) have been utilized in spectroscopy for detection of chemical agents, in active and passive imaging for detection of concealed weapons, radio astronomy, industrial controls, medicine, biotechnology, and in short range radars and secured high data rate communications [1]-[3]. The high cost and low level of integration of the devices have limited the proliferation of these applications. Recent progress in CMOS (Complementary Metal Oxide Silicon) integrated circuits (IC) technology has made it possible to consider CMOS as an alternative means for realization of capable and economical systems that operate at 200 GHz and higher. This paper discusses the performance of devices available in digital CMOS as well as those of signal sources and detectors operating between 100 and 800 GHz fabricated in digital CMOS, which suggest the feasibility of sub-millimeter wave operation of CMOS circuits.

II. Transistors and Diodes in CMOS

A. Speed Performance of NMOS Transistor

The consideration for CMOS based terahertz systems is made possible by the CMOS technology scaling. According to 2006 International Roadmap for Semiconductors (ITRS) [4], by year 2013, the projected NMOS unity power gain frequency (f_{max}) requirement is ~650 GHz. With such transistors, it will be possible to build an amplifier operating up to 300 – 350 GHz. However, there has been a great deal of concerns whether the CMOS technology scaling can continue. The reports of a bulk transistor from a 65-nm technology [5] with f_{max} of 420 GHz in 2006, and an SOI transistor from a 45-nm process with f_T of 450 GHz [6] in 2007 suggest that the industry has been able to keep up with the ITRS.

B. Schottky Diodes

In the near term, at frequencies higher than ~400 GHz, it will be difficult to achieve amplification using NMOS transistors. A way to deal with this is to use passive detectors and frequency multipliers (e.g. Schottky diodes) as routinely done for sub-millimeter systems [2]. It is possible to implement THz diodes in CMOS without any process modifications. Figure 1 shows the layout of a cell and a cross section. The Schottky contact is formed on a diffusion region with no source/drain implants. The ohmic contacts are placed on the n^+ implanted n-well. Such a diode with a $CoSi_2$-silicon Schottky junction has been realized in a 130-nm CMOS process [7]. The Schottky contact area is set at the minimum to maximize the cutoff frequency. This type of diodes can also be used for frequency multiplication to generate sub-millimeter wave signals [2],[8],[9].

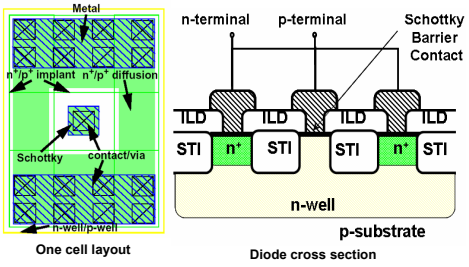

Figure 1. Integrated Schottky diode.

A diode formed using sixteen 0.32x 0.32μm^2 cells connected in parallel (R_s=13 Ω and C=8 fF) has measured f_T of ~1.5 THz. With further optimization, it will be possible to increase f_T to ~2 THz and operate detectors above 500 GHz.

III. Signal Generators

A. Fundamental Mode Voltage Controlled Oscillator (VCO)

Figure 2 shows the schematic of 140-GHz VCO fabricated in a 90-nm logic CMOS process [10]. It employs LC-resonators. Cross-coupled NMOS transistors (M_1, M_2) form

the VCO core. Inductors (L_1, L_2), accumulation mode MOS capacitors/varactors (C_1, C_2), and the capacitances associated with M_1 and M_2 form the LC resonators. The inductors, L_1 and L_2, are built using a single loop circular inductor. The diameter of circular inductor is 31.6 μm and the inductance of loop is around 65 pH. The VCO utilizes lumped elements which are more compact and higher Q than those based on transmission lines [11].

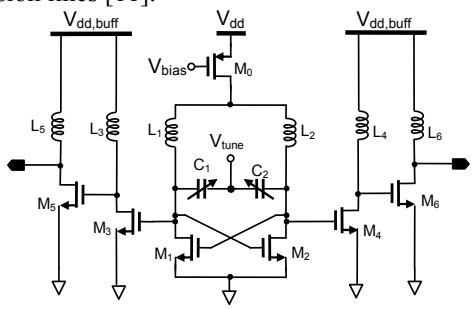

Figure 2. Schematic of 140-GHz Voltage controlled oscillator

The output frequency can be tuned from 139 to 140.2 GHz by changing the varactor voltage and bias current [11]. The measured output power is ~-19 dBm. The measured phase noise is ~-85 dBc/Hz at 2-MHz offset from the carrier. The tuning range is limited because the design is targeted for high operating frequency.

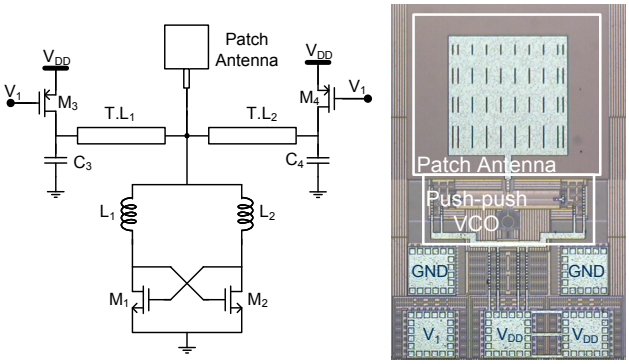

Figure 3. Schematic and photograph of a 410-GHz push-push VCO in 45-nm CMOS.

B. Push-Push VCO

Figure 3 shows the schematic of 410-GHz push-push VCO [12] fabricated in 45-nm CMOS. The push-push VCO [12]-[18] is based on the fundamental mode oscillators similar to the 140-GHz VCO. At the virtual ground nodes, the anti-phase fundamental signals cancel out and the second harmonic signal can be extracted. The middle point of inductors L_1 and L_2 has the parasitic capacitance to ground with the lowest value and highest Q among the common-mode nodes. This makes the impedance at resonant frequency the highest and the best port to extract the push-push output [17]. A quarter wavelength transmission line tuned for the second harmonic frequency is usually used to increase the amplitude of second harmonic while suppressing the fundamental signal [12],[17].

The transmission line is formed using a grounded coplanar waveguide (GCPW) structure. Compared to the conventional CPW, the ground plane isolates the line from the lossy silicon substrate and reduces the insertion loss. The lines are formed using the top bond pad metal layer and the ground plane is formed by shunting metal1-5 layers. The chip occupies 640 μm x 390 μm including the bond pads. The die photograph is also shown in Figure 3.

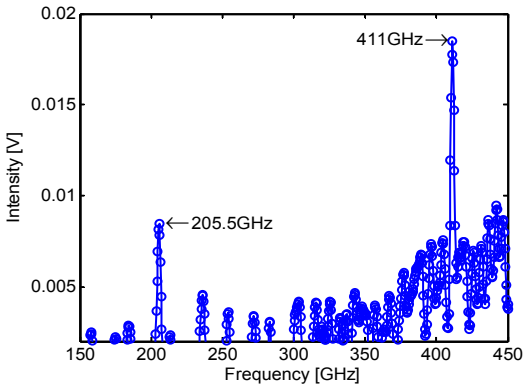

Figure 4. Output spectrum of the 410-GHz push-push VCO.

Measurements of ~400-GHz oscillator output are challenging. Presently, there are no commercially available electronic probes for measurements at this frequency. Because of this, an optical technique is utilized. To enable this, an on-chip patch antenna with an area of 200 x 200 μm^2 is integrated with the oscillator. The patch like the GCPW is formed using the bond pad metal layer while the ground plane is formed with metal1-5 layers shunted together. The patch and ground plane are separated by a ~4 μm thick SiO_2 layer. The relatively thin gap reduces the efficiency of antenna to ~ 20%.

The VCO spectrum is measured using a Bruker 113V FTIR system. The power level was measured using a silicon bolometer (HD-3, 1378) from Infrared Laboratories. Fig. 4 shows an output spectrum. The measured signal level is -49 dBm for the signal at 411 GHz. The circuit consumes 17 mW. The power level is low. This is mostly due to the losses associated with the transistor and thin metal layers available in the CMOS process and the mismatch between the tuned frequencies of patch antenna and oscillator. The output frequency of 410 GHz is the highest frequency for signals generated using transistors in any semiconductor technology.

C. Frequency Generation based on Linear Superposition

The push-push technique is a form of linear superposition technique using in-phase and 180^o out-of-phase signals to generate a 2^{nd} order harmonic signal. An *n*-th order harmonic signal can be generated using superposition of *n* signals with phase offsets of $360^o/n$ [19]. By linearly superposing quadratures of 81-GHz signals generated in a quadrature VCO using transistors M_9-M_{12} in Figure 5, 4^{th} order harmonic at 324 GHz is generated in a 90-nm CMOS technology [20]. The

output power is -46 dBm at 12 mW dc power consumption. The tuning range is 4 GHz and extrapolated phase noise is -91dBc/Hz at 10 MHz offset. Using this technique with 45-nm CMOS should yield output signals at ~800 GHz.

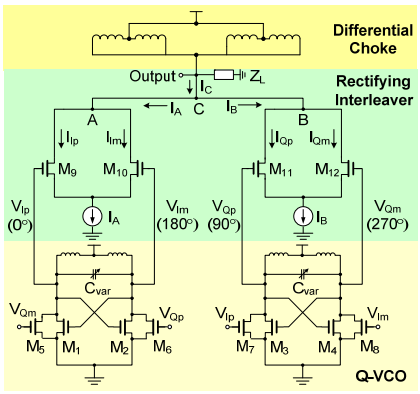

Figure 5. Frequency quadrupling VCO that linearly superposes quadratures of 81-GHz signals to generate 324-GHz signal in 90-nm CMOS.

D. Phase Locked Loop

Generation of free running high frequency signal by itself is not sufficient. The signal must be stabilized using a phased locked loop (PLL). A fully integrated PLL tunable from 45.9 to 50.5 GHz, which also outputs the second order harmonic at frequencies between 91.8 and 101 GHz, has been demonstrated in a 130-nm logic CMOS process [21]. Figure 6 shows a block diagram of the 50-GHz PLL.

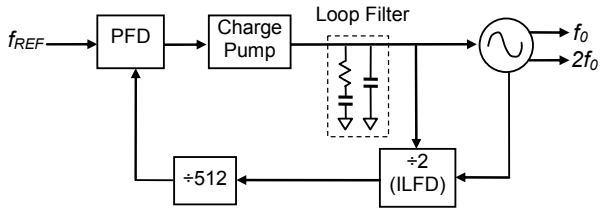

Figure 6. 50-GHz phase locked loop block diagram.

The circuit utilizes an injection-locked frequency divider (/2) (ILFD) for the first divide stage to achieve the 50-GHz operation. The injection locked divider is an LC-tank type [22], which is essentially an oscillator running near the half frequency of that for the VCO. The output power level of VCO is about -10 dBm and the phase noise of free running VCO is about -90 and -109 dBc/Hz at 1-MHz and 10-MHz offset from the carrier, respectively. The measurements are made at 1.5-V V_{DD} and 12-mA bias current. Figure 7 shows the locked spectrum of 2nd harmonic near 100 GHz.

Usually, the first frequency divider limits the maximum PLL operating frequency. Since, the divider is an oscillator whose operating frequency is lower than that of the VCO, the PLL maximum operating frequency is limited by the maximum VCO frequency. This means it should be possible to lock the 410-GHz signals in 45-nm CMOS.

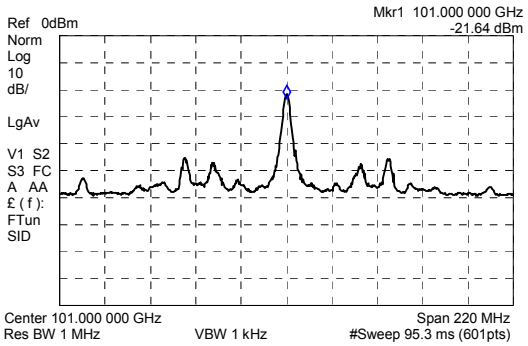

Figure 7. Measured PLL second harmonic output ~100 GHz.

IV. Detector Circuits

A 182-GHz Schottky diode detector was fabricated using 130-nm foundry CMOS [23]. The detector test signal was generated on-chip by modulating the bias current of a push-push VCO. As shown in Figure 8, the detector consists of an ~180-GHz RF matching circuit, Schottky diode, low pass filter with ~10-GHz corner frequency, and amplifier for driving a 50Ω load. The diode has been forward biased (0.3 mA) through a 1-kΩ resistor (R3). The detector input is conjugately matched to the on-chip test signal generator output at ~180GHz. Figure 9 shows the voltage waveforms of modulation and detected signals across a 50-Ω load, when the VCO is modulated with 10-MHz 0.1-V amplitude input signal at 1.75-V V_{DD}. The chip size is 1120 x 600 μm^2 including bond pads.

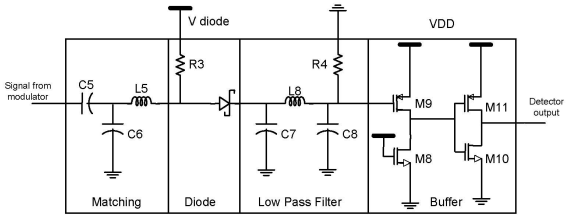

Figure 8. Detector schematic.

Sub-millimeter wave signals can also be generated and detected by exciting plasma waves (i.e. waves of electron density) in the CMOS channel. A ballistic transistor channel forms a resonant cavity, and drain current flow leads to the instability of plasma waves called Dyakonov-Shur instability [24]. Rectification of THz radiation by plasma related nonlinearities has been used for THz detection. This detection modality could support operation above10 THz.

Figure 10 shows the noise performance of 780-GHz plasma wave detector using an NMOS transistor of a 130-nm CMOS process [25]. The responsivity is greater than 200 V/W. The minimum power of signal with 1-Hz bandwidth that can be detected is around 100 pW for a detector using an NMOS transistor with width and length of 10μm and 300nm. This type of detectors has been utilized to build a terahertz camera [26].

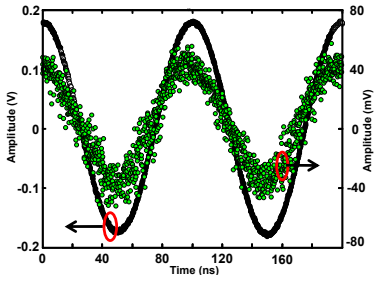

Figure 9. Measured 10-MHz modulation input signal compared to detector output signal.

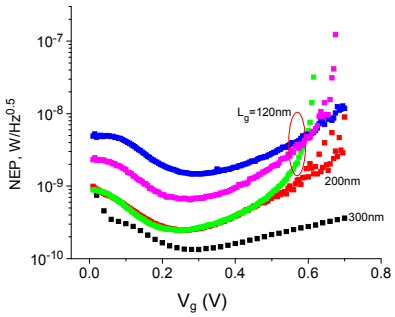

Figure 10. Noise equivalent power as a function of the gate voltage, V_g for Si MOSFETs of different gate lengths, T=300K.

V. Conclusions

Feasibility of using a mainstream foundry logic CMOS process to fabricate a signal generator and a detector that operate 200-800 GHz has been demonstrated. Use of linear superposition in oscillators should enable generation of ~800 GHz signals in 45-nm CMOS. The long term prospect is even more exciting. According to the 2006 International Roadmap for Semiconductor, by 2018, the required f_T and f_{max} of NMOS transistors in production are 0.7 and ~1 THz [4]. Such transistors will provide greater flexibility to implement and improve circuits and systems operating near 1THz.

Acknowledgement

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