A V-band Self-Healing Power Amplifier with Adaptive Feedback Bias Control in 65 nm CMOS

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Abstract **— A self-healing two-stage 60 GHz power amplifier (PA) with amplitude/phase compensation is realized in 65 nm CMOS. An adaptive feedback bias scheme with three control knobs is proposed to extend the linear operating region and enhance chip-to-chip performance yield; allowing a 5.5 dB improvement of the output 1-dB compression point (P_{1dB}) and a less than 2% chip-to-chip gain variation. At a 1 V supply, the fully differential PA achieves a saturation output power (P_{sat}) of 14.85 dBm with a peak power-added-efficiency (PAE) of 16.2%. With the on-chip amplitude compensation, the P_{1dB} is extended to 13.7 dBm. With the on-chip phase compensation, the output phase variation is minimized to less than 0.5 degree. To the best of our knowledge, this PA provides the highest P_{sat} and P_{1dB} with simultaneous high PAE for a single PA reported to date. The PA delivers a linear gain of 9.7 dB and has a 7 GHz bandwidth from 55.5 to 62.5 GHz with a very compact area of 0.042 mm^2.**

Index Terms **— CMOS, millimeter wave integrated circuits, power amplifier, transformers, V-band.**

I. Introduction

Multi-Gb/s short-range wireless applications at 60 GHz require high-yield, linear PAs to meet both low cost and stringent RF linearity specifications. As device size continues to scale down, process variations become significant and deteriorate the design-for-manufacturability (DFM) of high performance PAs. To concurrently solve the problems of yield and linearity, this paper presents a new concept of tunable self-healing output profile with feedback control that adjusts its output profile in response to process variations and linearizes the AM-AM profile as shown in Fig. 1. This unique aspect of PA design has not been reported in recent publications [1-8].

The nonlinear transconductance and temperature-dependent mobility of deep-scaled CMOS often result in early gain compression in PAs. This leads to a soft gain profile which has a large separation between P_{sat} and P_{1dB} that severely limits the linear operating range under a constrained supply voltage. Extending P_{1dB} can fully utilize the limited supply voltage to maximize the linear power region, thus increasing the transmitted power while satisfying the spectrum and constellation requirements.

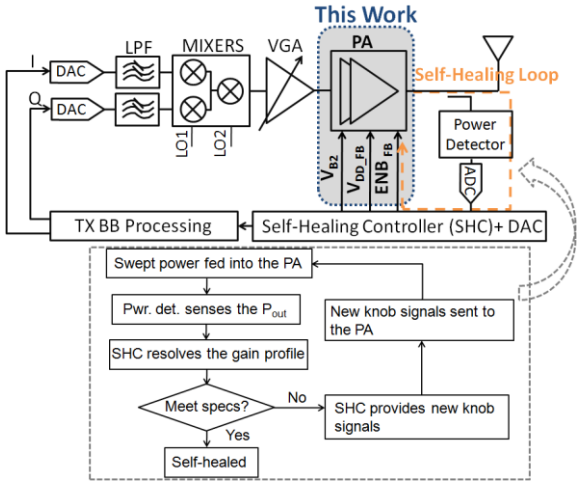

Fig. 1. Self-healing transmitter block diagram and flow chart.

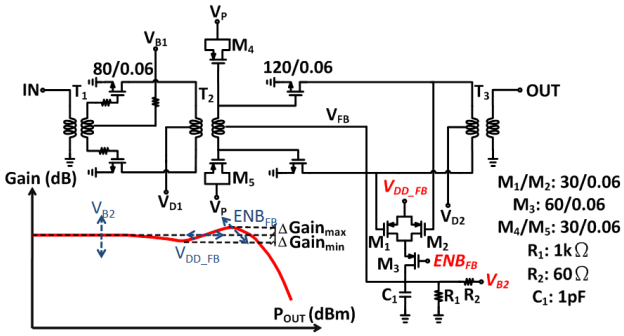

Fig. 2. Schematic of the 2-stage PA.

Our novel feedback structure enables this feature. This proposed architecture demonstrates the first high performance linear CMOS PA with amplitude and phase compensation, and simultaneous performance yield improvement with only 2% chip-to-chip gain variation.

II. Self-Healing Power Amplifier Design

A two-stage PA is designed for high output power, high efficiency and high linearity with a compact size. This PA is a fully differential transformer-coupled design in 65 nm 1P6M standard CMOS process as shown in Fig. 2. This process offers six metal layers with one thick top metal for low-loss passive design and interconnects.

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Fully differential configuration is chosen to minimize the interferences to other blocks, lower the even-order harmonics, and reject common-mode noise. The two stages are both designed with the common source topology to maximize voltage headroom under a limited power supply. Resistors are added at the gate of the first stage to stabilize the amplifier. The amplifier is biased at class-AB region to balance gain, power and efficiency.

This design utilizes transformers to provide a compact impedance matching and a simple biasing scheme applied at the center-taps. The high-pass characteristic of the transformers ensures stability at low frequencies. At input and output, the transformers convert single-ended signals to differential ones and vice versa to simplify testing complexity. The width of the input transformer (T_1) is relatively narrow (4 μm) to minimize the coupling capacitance from coils to substrate to maximize the self-resonant frequency. Both the primary and secondary coils are implemented on the top metal to maximize the quality factors. The width of the inter-stage and output transformers (T_2 and T_3) is wider (10 μm) to match with large devices in the last stage and to provide sufficient current-handling capability (> 100 mA). Because of its large size, a vertically-stacked transformer is adopted for a compact design. Stabilizing resistors are inserted at the center-taps of the transformers to improve the common-mode stability.

In order to maximize the linear operating power range, a novel feedback bias control loop (M_1–M_3, R_1, R_2, C_1) with small area (0.5%) and power (1%) overheads is applied to the last stage to dynamically adjust its gate bias V_{FB} according to the output power level. Low-threshold PMOS devices (M_1/M_2) are connected to the last stage to sense the output voltage. These two transistors have negligible effect on the PA performance due to their small loading imposed on the PA. Depending on the sensed output voltage swing, the feedback loop adjusts the gate bias of the last stage in real-time. The physical size of the feedback transistors (M_1/M_2) sets the range and the rate of change in the feedback bias V_{FB}. The optimal V_{FB} curve is first acquired from simulation to minimize DC power consumption in the low power region and adaptively increase the gain while power increases. The sizes of M_1/M_2 are selected accordingly so that the feedback bias matches the optimal one from simulation. A 1 pF capacitor (C_1) is inserted to filter the high frequency components. By properly selecting the parameters of R_1, R_2, and C_1, the bandwidth of the loop can be set higher than that of the signal envelope. Therefore, the dynamic gate voltage can promptly track the input signal envelope.

Three voltage control knobs, V_{DD_FB}, ENB_{FB}, and V_{B2}, shape the gain profile in three different aspects as indicated in Fig. 2. At low input power, the feedback transistors are off, and the gate voltage V_{FB} is set by V_{B2} and the resistor network (R_1 and R_2) at a low level to optimize efficiency. The linear gain is determined by V_{B2}. As the output voltage swing becomes larger than the threshold voltage of the feedback transistors, the feedback loop turns on and controls V_{FB}. Transistor M_3 acts as an enabler of the loop. Tuning the gate voltage of M_3 (ENB_{FB}) adjusts the feedback factor that determines the amount of the gain expansion $\Delta\,Gain_{max}$. V_{DD_FB} controls the triggered power where the feedback action occurs by changing the threshold voltage of the feedback transistors. V_{FB} starts at 0.45 V in the small-signal region and eventually increases to 0.75 V in the saturation region. This loop does not create any stability issues because the poles of the loop are far below 60 GHz.

Besides amplitude distortion, phase distortion also affects signal linearity in CMOS PAs. A PMOS-based capacitance compensation is applied to heal phase distortion by choosing the sizes of the PMOS devices (M_4/M_5) to cancel the nonlinear NMOS capacitor C_{gs} in the PA [9]. The effects of including the PMOS devices are accounted for in the design by properly selecting the transformer T_2 such that there is no gain and power degradation.

III. Self-Healing Algorithm

In deep-submicron CMOS, process variation is the predominant cause of chip-to-chip performance variations that limit performance yield. The proposed PA in conjunction with a self-healing controller (SHC) and a power sensor (not integrated in this work) can overcome the limitations imposed by process and environmental variations as shown in Fig. 1. The controller receives the data provided by the calibrated power sensor at the PA output and returns three voltage knob signals, V_{DD_FB}, ENB_{FB}, and V_{B2}, to the PA. One can effectively shape the gain profile of the PA to simultaneously overcome process variations and gain compression to meet the linearity specifications by tuning these knobs. The proposed healing algorithm as shown in Fig. 1 is as follows:

(i) A low-power reference signal is generated and fed into the PA. By monitoring the calibrated output power, the self-healing engine can resolve the linear gain and optimize it by adjusting V_{B2}.

(ii) After the linear gain is healed, a power sweep is conducted to obtain the $\Delta Gain_{max}$ and $\Delta Gain_{min}$ as shown in Fig. 2. To avoid signal distortion and extend P_{1dB} closer to P_{sat}, both Δ values should be kept within a certain range (e.g. 1 dB). V_{DD_FB} can be adjusted to tune the location and the amount of

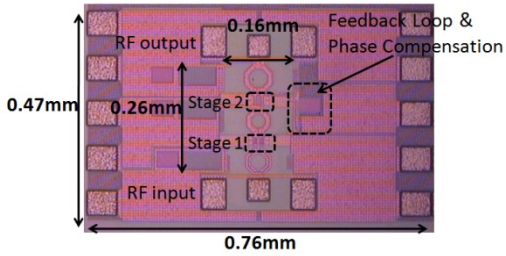

Fig. 3. Chip micrograph of the proposed PA.

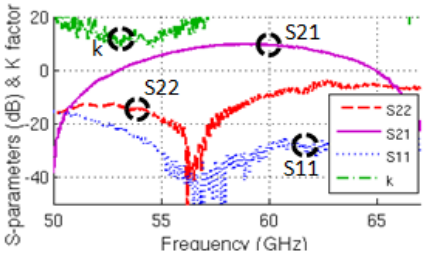

Fig. 4. Measured S-parameteres of the PA.

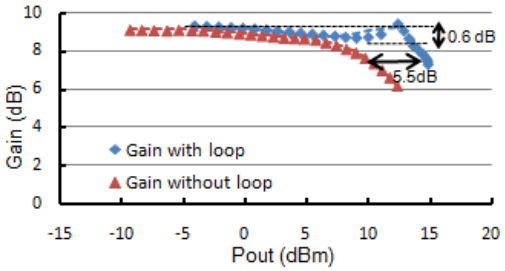

Fig. 5. Measured gain of the PA with and without the loop.

the gain expansion. It should be chosen that $\Delta Gain_{min}$ is less than 1 dB.

(iii) ENB_{FB} is tuned to adjust Δ $Gain_{max}$.

IV. Measurement Results

The chip micrograph of the PA is shown in Fig. 3. The PA occupies a compact area of 0.76×0.47 mm^2 including the pads.

The measured S-parameters are shown in Fig. 4 with a peak linear gain of 9.7 dB at 59 GHz. The 3-dB bandwidth is 7 GHz from 55.5 GHz to 62.5 GHz. The stability factor K larger than one across the entire spectrum demonstrates unconditional stability.

Single-tone large-signal performance of the PA is performed by a V-band source module HP 83557A and an Agilent V8486A V-band power sensor. To show the effectiveness of the feedback control loop, a PA without the loop is fabricated for comparison. Fig. 5 shows the gain profiles of the PAs with and without the loop operated at a 1 V supply. In the small-signal region, both PAs have the same linear gain. As the input power increases, the PA without the feedback loop starts to compress because of the limited maximum current, whereas the one with the loop remains relatively constant until it experiences expansion before its eventual compression. The gain of the PA with the feedback loop compresses by 0.6 dB and then expands by 0.1 dB relative to its small-signal level before it reaches P_{1dB}. The P_{1dB} differs by 5.5 dB between two PAs with and without the feedback bias control.

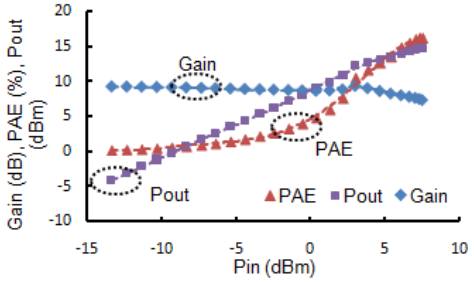

Fig. 6. Measured gain, output power, and PAE of the PA.

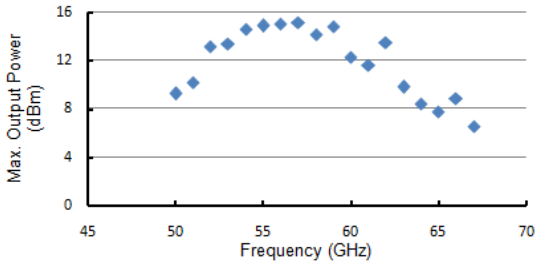

Fig. 7. Measured P_{sat} vs. frequency of the PA.

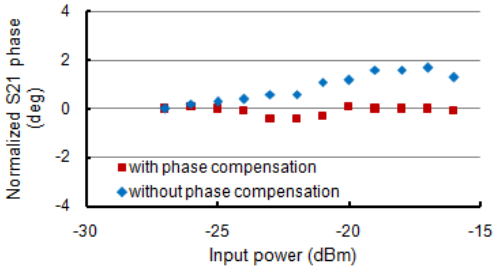

Fig. 8. Measured S21 phase with and without phase compensation.

The output power, gain, and PAE of the proposed PA are shown in Fig. 6. The P_{1dB} and P_{sat} of the PA with the feedback loop are 13.7 dBm and 14.85 dBm, respectively. The measured peak PAE is 16.2%. Fig. 7 shows the P_{sat} as a function of frequency. More than 10 dBm of P_{sat} is achieved from 52–63 GHz. P_{sat} measurement above 63 GHz is limited by the input signal from the V-band source.

The measured S21 phase is shown in Fig. 8. The S21 phase variation reduces from 1.7^o to 0.4^o by applying the on-chip PMOS-based phase compensators.

Two CW signals at 59 GHz and 59.1 GHz are applied to the input of the PA to measure its third-order intercept

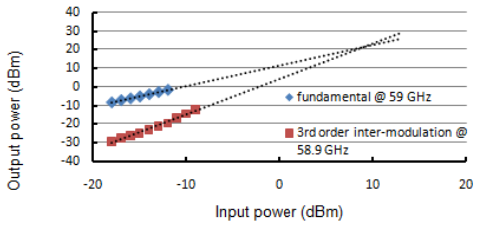

Fig. 9. Measured two-tone performance of the PA.

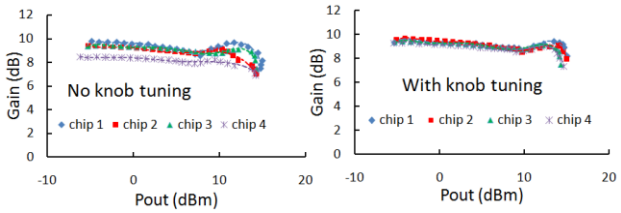

Fig. 10. Measured gain with and without healing.

point. The measured fundamental tone at 59 GHz and the third-order inter-modulation tone at 58.9 GHz are shown in Fig. 9. The extrapolated output third-order intercept point is 20.4 dBm.

To demonstrate the self-healing concept, four chips are measured by controlling the three knobs externally. The results are shown in Fig. 10. Before applying the healing algorithm, three control knobs are biased at fixed voltages and the gain profiles show variations in both small- and large-signal regions. After externally controlling the three knobs as described in section III, the four chips show a significantly reduced gain variance of 2%, as compared to 22% before healing.

V. Conclusion

A V-band self-healing PA with adaptive feedback bias control using 65 nm CMOS process is designed and demonstrated. With the proposed on-chip tunable output profile technique, the linear operation region is effectively extended by 5.5 dB. This compact PA achieves large output power, high linearity and high PAE simultaneously. It delivers a P_{sat} of 14.85 dBm and a P_{1dB} of 13.7 dBm with 16.2% peak PAE. Table 1 summarizes the performance of this PA with the highest figure-of-merit=69.6 (defined by $PAE*P_{sat}/(P_{sat}-P_{1dB})$) that compares favorably to previously published V-band PAs. The measured results from four chips demonstrate the self-healing capability of the PA in improving performance yield by algorithmically adjusting the control knobs. The PA validates a self-healing concept and provides a highly-linear and high-performance-yield solution for applications in the spectrum-efficient digital communication systems.

TABLE I
Comparison of 60 GHz Silicon PAs

	This work	[1]	[2]	[3]	[4] ※	[5]	[6]	[7] ※	[8]
Technology (nm)	65	45	65	90	90	65	65	65	65
V_{DD} (V)	1	1.1	1	1	1	1.2	1.2	1.2	1
Gain (dB)	9.4	6	15.8	10	4.2	13.7	8.5	14.3	30
P_{sat} (dBm)	14.85	13.8	11.5	12.6	14.2	14.2	7.2	16.6	10.6
P_{1dB} (dBm)	13.7	11	2.5	8.8	12.1	12.2	4.2	11	6.8
Peak PAE (%)	16.2	7	11	6.9	5.8	8.4	2.3	4.9	18
Area (mm^2)	0.042	0.05	0.05	0.64 *	1.19 *	1.2 *	0.06	0.46*	0.05
PAE @ P_{1dB} (%)	13.5	6 #	5 #	< 5 #	< 5 #	n/a	n/a	< 5 #	7.7
Phase compensation	Yes	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
$PAE*P_{sat}/(P_{sat}-P_{1dB})$	69.6	14.7	12.6	11.8	15.1	22.8	4.6	6.8	35.3

※ Including pads
Estimated from figures
FoM: $PAE(\%)*P_{sat}(mW)/(P_{sat}-P_{1dB})(mW)$
* power combining

Acknowledgement

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