A CMOS Fully Differential W-Band Passive Imager with <2 K NETD

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***Abstract* —This paper presents a fully differential W-band passive imager that integrates LNA, Dicke switch, detector and filter, with minimum NEPs of 21 $fW/\sqrt{Hz}$ / 24 $fW/\sqrt{Hz}$ for without/with switch cases and a peak responsivity of >1.8 MV/W. To authors' knowledge, this represents the largest responsivity to date from a CMOS radiometer chip. It achieves NETD = 1.94 K with 30ms integration time. The chip occupies 0.49 mm^2 active area with 57 mW power consumption.**

***Index Terms* — CMOS, Differential, Passive Imager, W-band.**

I. Introduction

Millimeter/sub-millimeter wave imaging draws increasing interest due to its uniqueness in seeing through fabric/fog, reflecting off the metal and spectrally sensitive to critical chemicals, which holds high promise in applications of remote terrestrial/atmospheric sensing, public security and medical related imaging systems [1]. Passive imaging is particularly preferable in comparison with its active counterpart because it does not need power-hungry transmitters at mm-Wave frequencies and does not comply to FCC or other regulations. However, passive imaging requires substantially better sensitivity due to weaker receiving signals. Today's mm-wave passive imaging systems are mainly based on exotic technologies, such as InP HBT/HEMT, GaAs, etc., which are discrete and expensive for system implementation [2, 3].

To realize a single chip imager with small form factor and low power consumption, researchers are actively working on silicon based solutions. Ref. [4] demonstrated a 94 GHz LNA + Detector circuitry in SiGe for passive mm-Wave imaging with noise equivalent power (NEP) of 21 $fW/\sqrt{Hz}$. To validate CMOS capabilities, Ref. [5] implemented a 90 GHz passive imager in 65nm CMOS process, with NEP of 0.11 $pW/\sqrt{Hz}$ NEP and responsivity of 63 kV/W. Ref. [6] explored Schottky diode in CMOS technology with a NEP about 40 $pW/\sqrt{Hz}$. Ref [7] further integrated the baseband into a passive imager in SiGe process to achieve the capability of 0.3 K or 0.4 K noise equivalent temperature difference (NETD) with integration time 40 ms or 30 ms, respectively. All these research efforts are contributing to the goal of silicon based integrated passive imagers.

This work intends to realize a CMOS based differential passive imager for portable system applications. CMOS implementation not only offers the highest integration level and lowest cost, but also improves the system yield with the aid of on-chip digital signal processing. However, CMOS technology has its inherent shortages, such as lossy substrate, low quality factor Q of devices, flicker noise, etc., which requires novel system structure and creative circuit design ideas. This paper will present a CMOS based imager structure and demonstrate the prototype of RF/analog circuits with integrated Dicke switch to reduce detrimental flicker noises and circuit gain variations for high sensitivity passive imaging applications.

II. System Description

A. Passive Imager Architecture

One of the most critical metrics in passive imagers is the noise equivalent temperature difference (NETD), which determines the image resolution and performance [8], as shown in Eq.(1),

$$NETD = T_{SN}\sqrt{\left(\frac{1}{B\tau}\right)+\left(\frac{\Delta G}{G}\right)^2} \qquad (1)$$

which specifies that NETD is inversely proportional to receiver front-end bandwidth B, front end gain G, integration time τ, and proportional to gain variation ΔG, system noise equivalent temperature T_{SN}. To reduce the response time or integration time τ, and improve the temperature resolution, low noise and wide bandwidth are two important aspects. Besides, the gain variation ΔG is also critical in CMOS technology due to its higher flicker noise and larger process variations. To minimize ΔG effects, Dicke switch [9] can be used to sample and cancel gain variations by alternatively reverse the polarity and average over time. By making the Dicke switch operation clock frequency higher than the flicker noise corner, the flicker noise effects can be substantially alleviated.

Figure 1 presents the proposed passive imaging RF/analog front end, which includes an input balun, differential LNA and detector with on-chip Dicke switch. Fully differential architecture is chosen to suppress common mode and supply noises at the cost of extra power consumption. Single-ended input and output signals

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are chosen to facilitate the testing. The input balun serves as the conversion from single-ended to differential signals as well as input matching. The Dicke switch and integration will calibrate gain variations and circuit inherent flicker noise. NETD can therefore be represented as Eqn. (2) by eliminating the gain variation ΔG effects [4]. The factor 2 accounts for the factor that only half of the period is used to detect the signal.

$$NETD = 2 \times \frac{NEP}{kB\sqrt{2\tau}} \qquad (2)$$

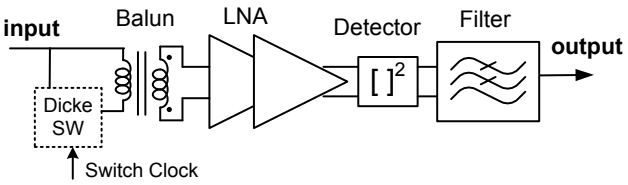


Figure 1 CMOS passive imaging with fully differential implementation and integrated Dicke switch

B. Circuit Design Description

LNA is the first stage of the receiver, which is critical to achieve low noise and high gain for high sensitivity imager with needed temperature resolution. Figure 2 sketches the LNA schematic, which features four-stage amplification and adopts fully differential, common source cascode structure. Transformer based inter-stage coupling and matching are utilized for compact implementation. Cascode structure benefits amplifier stability through input and output isolation. However, the node between amplification and cascade transistors has large parasitic capacitance, which greatly degrades the gain performance due to a large portion of shunt current to ground. To alleviate that effect, series transmission line is inserted to tune out the parasitic capacitance. Different from prior arts single ended implementation [4,5,7], the fully differential structure is more suitable for SoC integration due to its high immunity to supply and common mode noises.

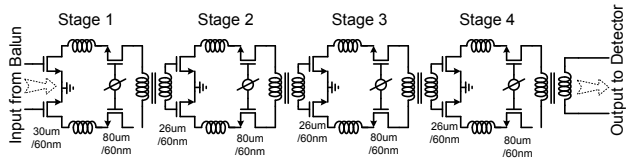


Figure 2 Schematic of differential LNA

To overcome MOS flicker noise that is much larger than the black body radiated input signal, chopper is mandatory to be integrated. This W-band imager utilizes Dicke switch to alternate between input signal and a known fixed reference to calibrate out circuit noises and gain variations due to the shared signal path. Therefore, the switch should position at the very front to incorporate all possible circuit noises, which locates before LNA input. Of course, it demands a very small switch insertion loss for minimum performance degradation. Fig. 3 (a) shows the proposed switch circuit and simulated insertion loss, which demonstrates the best performance to-date compared with that of state-of-the-arts [9]. Fig. 3(b) animates the working mechanism. The top figure represents the period during signal detection, and the bottom one illustrates the reference calibration cycle. This switch inserts no active device along the signal path. It thereby minimizes the insertion loss and eliminates extra parasitics, which otherwise would jeopardize the input tuning by loading the input signal path.

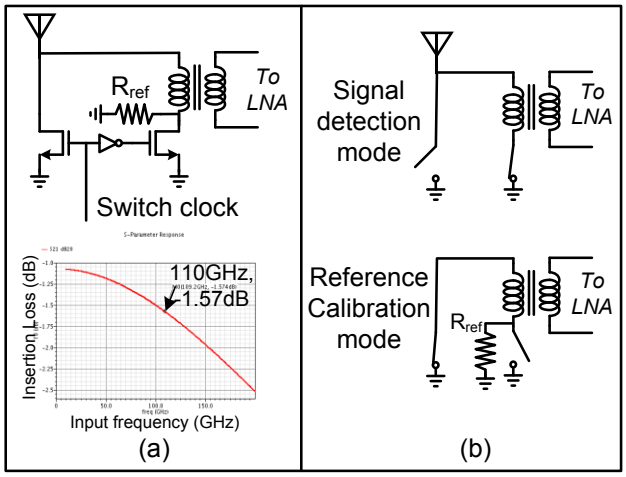


Figure 3 (a) Dicke switch schematic and simulated insertion loss; (b) Signal detection and reference calibration modes

III. Measurement Results

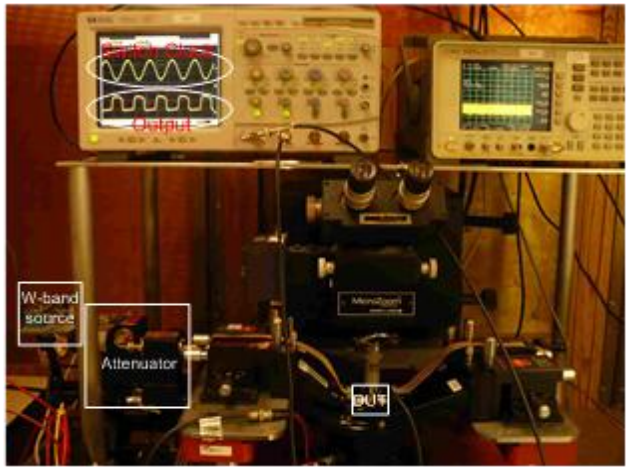
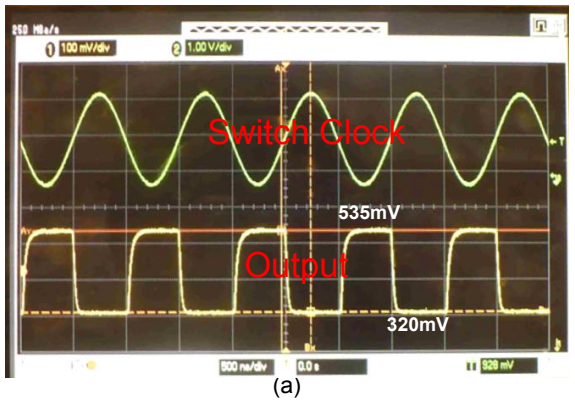


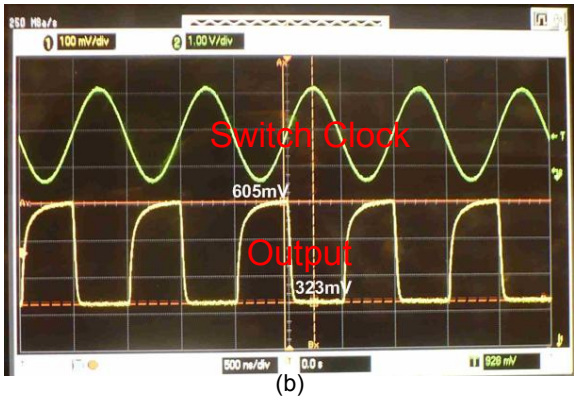
Figure 4 Measurement setup

Figure 4 shows the measurement setup. Monolithic multiplier chain generates W-band signal, which passes

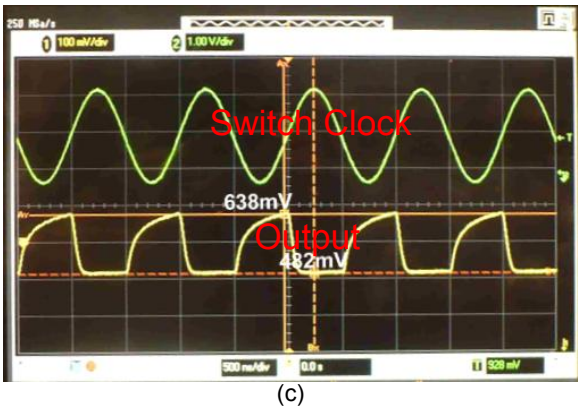
through the external attenuator to feed into the chip input. The attenuator is with 100 dB dynamic range and used to adjust the input signal strength to facilitate the characterization. A spectrum analyzer is used to debug the measurement setup and an oscilloscope is used to measure the W-band imager outputs, which is chopped by the Dicke switch clock at around 1 MHz. The output and switch clock are shown in the oscilloscope with top sinusoidal signal as the switch clock and bottom square-like signal as the circuit output. The switch clock troughs correspond to signal detection periods, and the switch clock peaks align with reference calibration periods.



(a)



(b)



(c)

Figure 5 Output signal versus different input power; (a) small input; (b) medium input; (c) large input

Figure 5 (a-c) illustrate the output waveforms at different input power levels. Top sine wave single is the Dicke switch clock, bottom square-like signal is the imager output denoting the measured signal strength. The output high DC level indicates signal level and the low DC level indicates noise. As shown in Fig. 5(a), high DC level is about 535 mV, low DC level is about 320 mW for a small input. As the input signal power increases, the high DC level increases initially with the low DC level remain unchanged. As shown in Fig. 5(b), high DC level increases to 605 mW and low DC level is still about 320 mV. When the input power further increases, high DC level reaches the highest level due to circuit saturation; and the low DC level corresponding to reference calibration period starts increasing so that the swing reduced, shown in Fig. 5(c), until it saturates to the same highest DC level. The reason that low DC level increases at high power input is because the Dicke switch could not completely isolate the external input during reference calibration period so that small portion of input leaks into the receiver during calibration periods. Therefore, output amplitude increases initially versus input then decreases due to the signal saturation and finally the output settles into a straight line.

Figure 6 shows the measured responsivity for these 2 cases: with and without Dicke switches. The measured peak responsivities with/without switch are 1.8 MV/W and 2.1 MV/W, and average responsivities are 1.15 MV/W and 1.5 MV/W over 99~111 GHz respectively. Figure 7 shows the measured NEPs for both without and with switches: by measuring the output noises at 1 MHz offset without switch and 1.5 MHz offset with switch at 1MHz switching rate. The measured minimum NEPs are 24 $fW/\sqrt{Hz}$ and 21 $fW/\sqrt{Hz}$ and average NEPs are 39 $fW/\sqrt{Hz}$ and 29 $fW/\sqrt{Hz}$, respectively. It also validates the insignificant performance degradation caused by the proposed Dicke switch. By equation (2), the noise equivalent temperature difference NETD is 1.94K with 30ms integration time.

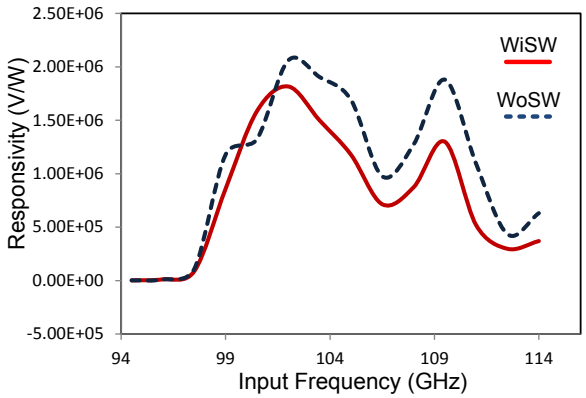


Figure 6 Measured responsivities for both with and without switch cases

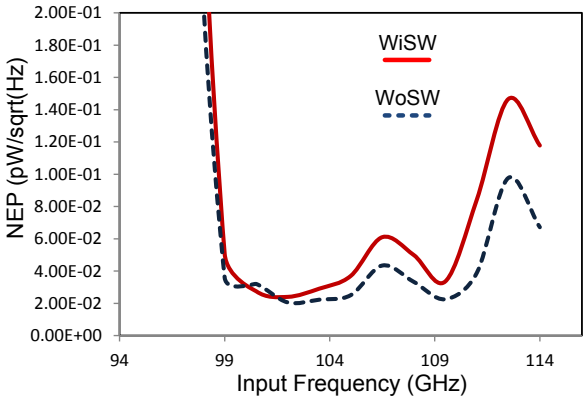


Figure 7 Tested NEPs: by measuring the output noises at 1 MHz offset without switch and 1.5 MHz offset with switch at 1 MHz switching rate.

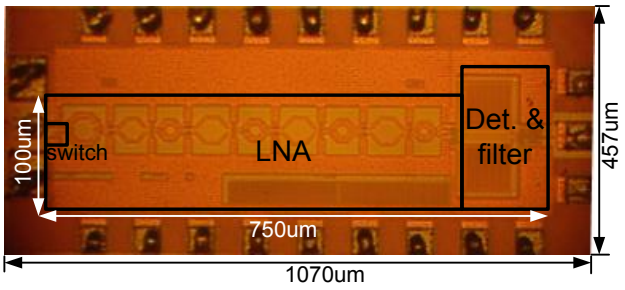


Figure 8 Die photo

Table 1 Performance summary and comparison with state-of-the-art silicon based implementations

	Ref.[4]	Ref.[5]	this work
Technology	0.12um SiGe	65nm CMOS	65nm CMOS
Architecture	Single-ended	Single-ended	Differential
NEP	21fW/√Hz	111fW/√Hz	39fW/√Hz
Responsivity	2.5~5MV/W	63kV/M	1.15MV/W
NETD with 30ms integration time	0.83K	12.5K	1.94K
Power	35mW	38mW	57mW

Table 1 summarizes the performance and comparison with that of the state-of-the-art silicon based implementations [4, 5]. The NETD with 30 ms integration time is about 1.94 K that demonstrates CMOS applicability in constituting the high resolution passive imaging system. Fig. 8 shows the die photo, which occupies 1.07 mm x 0.46 mm silicon area with pads and 0.75 mm x 0.1 mm without pads. The overall power consumption is 57 mW.

IV. Conclusion

This work realizes the first fully differential W-Band passive imager front-end with integrated Dicke switch. The measured minimum NEP is 24 $fW/\sqrt{Hz}$ and average NEP is 39 $fW/\sqrt{Hz}$ with the peak/average responsivities of 1.8 MV/W and 1.15 MV/W, respectively, which achieves to-date the highest responsivity in CMOS implementations. The NETD is 1.94 K with 30 ms integration time. This work further pushes the applicability of CMOS technology for portable passive mm-wave imaging systems with high integration, high resolution and low power operation.

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