A Compact 0.8-6GHz Fractional-*N* PLL with Binary-Weighted D/A Differentiator and Offset-Frequency Δ–Σ Modulator for Noise and Spurs Cancellation

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Abstract

A compact, low power and global-mismatch-tolerant 0.8-6GHz fractional-*N* PLL covers IEEE 802.11abg, PCS/DCS and cellular bands by using a binary-weighted 2nd order digital/analog differentiator (DAD) to achieve 2nd order mismatch shaping and reduce the quantization noise by 25dB, and using a 3rd order offset-frequency Δ–Σ modulator to reduce in-band spurs by 20dB in simulation and 8dB in current single-ended practice.

Introduction

As the wireless industry continues to grow, many portable devices are being designed to cover multiple standards at various frequency bands. Fractional-*N* PLL becomes indispensable owing to its ability to create fine frequency steps under various reference frequencies. Its fractional division is typically achieved by using the Δ–Σ modulator, and a wide loop bandwidth is preferably chosen to minimize VCO phase noise. Such designs, however, tend to expose PLL to broader quantization noise and/or fractional spurs, and inevitably encounter the following significant design issues:

- Effectiveness of quantization noise cancellation depends strictly on high charge pump (CP) linearity and low DAC mismatch. Techniques were proposed to shape the DAC mismatch [1-3], but all with constraints. For instance, the dynamic element matching (DEM) method demands extensive DSP to surmount mismatch effect due to process variation and often renders mismatch shaping to 1st order. The widely used thermometer-coded [1-2] or fully-segmented DAC [3] consumes either large routing area or twice the number of DAC units.
- Diminishing fractional spurs can only be accomplished by increasing CP linearity. A quantizer was proposed for suppression of fractional spurs [4]. The added noise, however, could not be rejected by high-pass function and degraded PLL's in-band SNR.

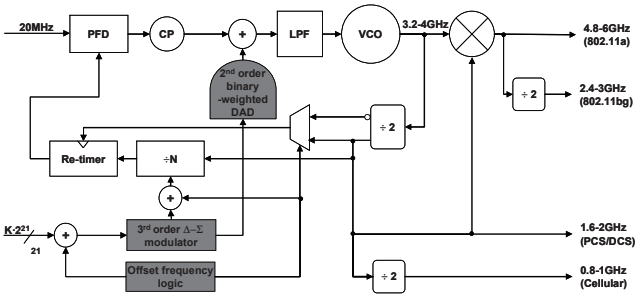


Fig. 1 Block diagram of 0.8-6GHz fractional-*N* PLL.

In this work, we apply two new techniques to mitigate above PLL design issues. A binary-weighted digital/analog differentiator (DAD) is used to obtain 2nd order mismatch shaping without DEM, and thermometer-coded or fully-segmented DAC. Additionally, a 3rd order offset-frequency modulator is used to alter the fractional frequency and prevent fractional spurs from falling in the loop bandwidth.

Binary-Weighted D/A Differentiator

Fig. 1 shows the proposed PLL. VCO operates from 3.2 to 4GHz, whose outputs are then up-converted to 4.8 to 6GHz and divided to 2.4GHz for the 802.11abg standards. Two cascaded divided-by-two circuits are added to cover PCS/DCS and cellular bands. With 20MHz reference and a 21-bit Δ–Σ modulator, fractional frequency step can be specified as $20/2^{21}$MHz. The detailed noise cancellation loop is revealed in Fig. 2(a). MASH-111 is used to form 3rd order Δ–Σ modulator and generate the unprocessed quantization error, e_3. Three differentiators are supposedly needed to obtain the noise cancellation signal, $e_3(1-z^{-1})^3$ and high-pass filter the truncation noise, e_6. But none of them is required in this implementation, because one can be functionally neutralized by a subsequent integrator, which imitates the PFD function in the cancellation path, and two others can be merged with four DAC elements to form a 2nd order DAD [5]. This unique arrangement saves the integrator and additional Δ–Σ modulator as compared with [1].

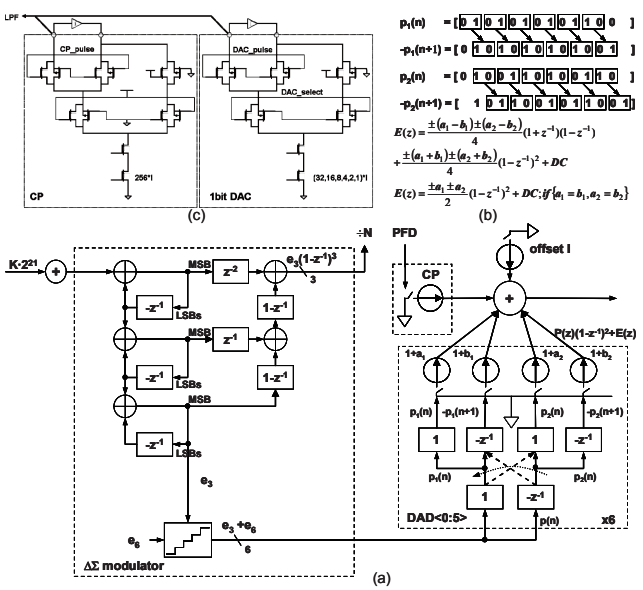


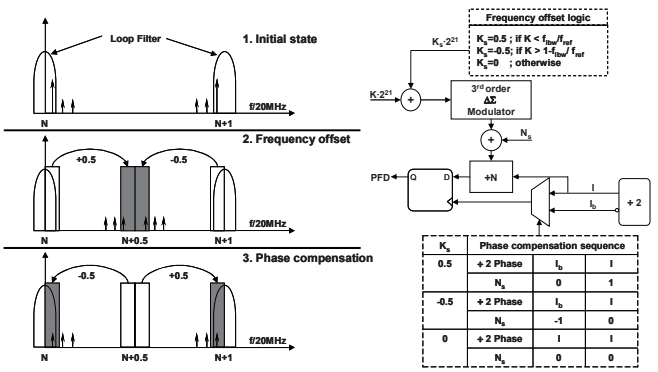
Fig. 2 2nd order DAD realization for quantization noise cancellation

Since the only possible values at DAC inputs, $[p_1(n), -p_1(n+1)]$ and $[p_2(n), -p_2(n+1)]$, are either [(0,1), (1,0)] or [(1,0), (0,1)], the error from the DAC mismatch, a_1, b_1, a_2 and b_2, can be estimated by using equations given in Fig. 2(b). The common-mode mismatch between adjacent elements of $(a_1+b_1)/2$ and $(a_2+b_2)/2$ will be filtered by $(1-z^{-1})^2$. Consequently, the 2nd order mismatch shaping can be realized as the differential-mode mismatch, $(a_1-b_1)/2$ and $(a_2-b_2)/2$,

between adjacent elements is minimized. The DAC matching requirement can therefore be relaxed to only local matching between adjacent DAC pairs, which are easy to route symmetrically with interdigitated technique without using complicated selection mechanism of prior arts to reduce global mismatches. The multi-bit DAD can also be implemented with binary-weighted architecture because gain error in each binary-weighted element can be treated as the common-mode mismatch and will be filtered by 2nd order high-pass function. Compared with the thermometer-coded (or fully-segmented) DAC with 1st order DEM, the 2nd-order binary-weighted DAD offers 20dB more mismatch reduction in simulation [5] and occupies smaller chip area. Additionally, an offset current pulse is added to enhance the CP linearity and compensate for unsigned DAD operation. The matching between CP and DAD can be attained with the same NMOS to replicate each other as shown in Fig. 2(c).

Offset-Frequency Δ–Σ Modulator

The CP non-linearity, caused by periodic erratic currents due to supply bounces and the finite transient time of current pulses, allows the fractional frequency (f_{fract}) to be sampled by the reference frequency (f_{ref}) and appear as fractional spurs within the loop bandwidth (f_{lbw}), when $f_{fract}<f_{lbw}$ or $f_{fract}>f_{ref}-f_{lbw}$. Dithering the Δ–Σ modulator LSB cannot totally remove fractional spurs because the coherence time of CP nonlinearity is longer than that perturbed by the dithering.



K_s	Phase compensation sequence		
0.5	÷ 2 Phase	I_b	I
		N_s	0	1
-0.5	÷ 2 Phase	I_b	I
		N_s	-1	0
0	÷ 2 Phase	I	I
		N_s	0	0

Fig. 3 Offset-frequency algorithm for fractional spurs cancellation

To mitigate this problem, an offset-frequency Δ–Σ modulator is utilized in Fig. 3 to shift fractional spurs beyond f_{lbw} by adding or subtracting 0.5 from the input of the modulator, depending on if f_{fract} is below f_{lbw} or above $f_{ref}-f_{lbw}$. This frequency shift, $f_{ref}/2$ or $-f_{ref}/2$, is offset later by re-synchronizing the divider output. To shift $-f_{ref}/2$ back, we use 180° phase delay signal to sample the divider output each cycle. This can be done by alternately sampling divider output with the inverted signal at one clock cycle and the N+1 divider at the next cycle. Similarly, shifting $f_{ref}/2$ can be realized by sampling the N-1 divider with the inverted signal every other cycle. The timing mismatch between two differential edges may introduce additional spurs. However, they appear only at $f_{ref}/2$, and far away from f_{lbw}, since timing mismatch presents only periodically every other clock cycle. By enabling this offset-frequency technique, we have observed at least 20dB fractional spurs reduction in simulation assuming the CP nonlinearity is a slow varying function over time.

Measurement Results and Conclusion

A prototype 0.8-6GHz PLL is fabricated in 0.18um CMOS process. The measured phase noise at 3.24GHz is shown in Fig. 4(a). When enabling DAD, the quantization noise is reduced by 25dB at the MHz range, which permits wider loop bandwidth (400KHz) to lower VCO phase noise. Compared with the integer-*N* operation, the residue quantization noise is only 3dB higher. In Fig. 4(b), fractional spurs at 133KHz offset appear as high as -42dBc. After enabling the offset-frequency technique, 8dB reduction is observed, which results in sufficiently low fractional spurs for intended multi-standard applications. Less spurs reduction than expected is caused by contaminated reference clock jitter from divider ground bounce and can be improved by isolating the crystal oscillator or utilizing differential circuits. The additional spurs from re-sampling appear at 10MHz offset, 66dBc below the main tone. Fig. 5 summarizes the PLL performance for different standards.

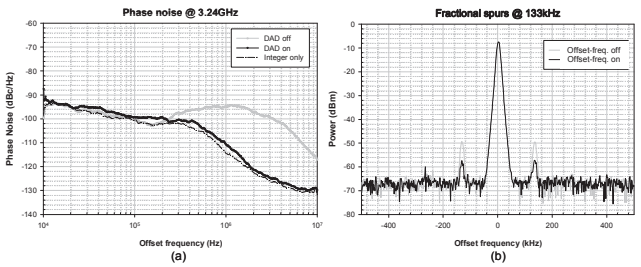


Fig. 4 (a) Noise and (b) spurs cancellation with proposed techniques

The chip area is 4mm^2 mostly occupied by on-chip loop filters and pads. The PFD/CP/DAD only occupies 0.08mm^2 and the modulus divider with Δ–Σ modulator occupies another 0.04mm^2. The total power consumption is 88.2mW under 1.8V supply. Excluding LO generators, the fractional-*N* PLL core consumes 24mA.

	Area (mm^2)	Current (mA)
VCO	0.25	8
LO generator	0.30	25
PFD/CP/DAD	0.08	10
Modulus divider /re-timer	0.01	4
ΔΣ modulator /digital	0.03	2

	Cellular	PCS/DCS	802.11bg	802.11a
Spot phase noise @100k (dBc/Hz)	-108	-103	-99	-92
RMS phase noise 10KHz~10MHz (°)	0.25	0.38	0.58	1.28
Fractional spurs (dBc)	-50*	-43*	-50	-44
Reference spurs (dBc)	-71	-64	-67	-62
* Offset-frequency technique is disable during the measurement				

Fig. 5 Performance Summary

References

[1] S. Pamarti, L. Jansson and I. Galton, "A wideband 2.4GHz delta-sigma fractional-N PLL with 1-Mb/s in-loop modulation," *J. Solid-State Circuits*, vol. 39, pp. 49-62, January 2004.

[2] S. Meninger and M. Perrott, "A 1-MHz bandwidth 3.6-GHz 0.18-µm CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *J. Solid-State Circuits*, vol. 41, pp. 966-980, April 2006.

[3] A. Swaminathan, K. Wang and I. Galton, "A wide-bandwidth 2.4GHz ISM-band fractional-N PLL with adaptive phase-noise cancellation," *ISSCC Dig. Tech. Papers*, pp. 302-303, Feb., 2007.

[4] K. Wang, A. Swaminathan and I. Galton, "Spurious -tone suppression techniques applied to a wide-bandwidth 2.4GHz fractional-N PLL," *ISSCC Dig. Tech. Papers*, pp. 342-343, Feb., 2008.

[5] H. Jian, Z. Xu and F. Chang, "Delta-sigma D/A converter using binary-weighted digital-to-analog differentiator for second order mismatch shaping," *Trans. Circuits Syst. II*, vol. 55, pp. 6-10, Jan. 2008.