# A Single-Channel 10b 1GS/s ADC with 1-cycle Latency using Pipelined Cascaded Folding 

Alireza Razzaghi, Sai-Wang Tam, Pejman Kalkhoran, Yu Wang, Chih-Yi Kuan, Brian Nissim, Lan Duy Vu, M.C. Frank Chang<br>UCLA, High Speed Electronics Lab, 64-127 Engr IV, Los Angeles, CA, 90095, USA


#### Abstract

A 10b 1GS/s ADC employing a single channel cascaded folding architecture is presented. Conversion speed of $1 \mathrm{GS} / \mathrm{s}$ is attained by incorporating low-power distributed track-and-hold amplifiers after each folder. This ADC achieves a record 55.6dB peak SNDR and a 64 dB peak SFDR and sustains a latency of one clock cycle. DNL and INL at 1GS/s sampling rate are measured 0.4 LSB and 1.1 LSB . Fabricated in a $0.35 \mu \mathrm{~m}$ BiCMOS process, the ADC consumes 2 W from a 3.5 V supply.

Index Terms - ADC, cascaded folding, folding, pipelined, SiGe BiCMOS process


## I. MOTIVATION

Military surveillance, airborne early warning, and target recognition systems are swift decision making applications that require high-speed, low-latency electronics. These systems employ high dynamic range Digital Radar Receivers (DRR) that place the ADC as close to the antenna as possible. This mandates the use of ADC architectures that achieve 810 bits of accuracy at GHz conversion rates.

## II. ADC ARCHITECTURE

Time-interleaved schemes lead to high conversion rates [1]-[2]-[3]-[4]. However, they are susceptible to timing misalignments [2]-[4] and limited linearity [1]-[2]-[3] prevalent in CMOS technologies. Moreover, the large latency associated with the conventional pipeline [1]-[3]-[4] and successive approximation architectures [2] hinders the use of such timeinterleaved schemes in high dynamic range DRRs.

An ADC is proposed which eliminates the timing misalignment by employing a single channel quantizer as depicted in Fig. 1. Since conversion speed is a premium, a cascaded folding scheme is adopted. Subranging, and multi-step schemes employ some form of decision feedback loop, limiting their ability to be scaled up in conversion speed. The superior matching of the BJTs lends itself to the cascaded folding scheme, therefore, a BiCMOS process is used to implement the ADC.

## III. CIRCUIT DESIGN

An open loop track-and-hold amplifier (THA) with enhanced linearity is designed to meet the wide


Fig. 1: Proposed ADC architecture.
dynamic range DRR specifications. Shown in Fig. 2, this THA is based on the design introduced in [5]. The input signal $V_{\text {in }}+$ is replicated at the collector of the diode-connected transistor $\mathrm{Q}_{\mathrm{d}}$ by experiencing an equal down-shift and up-shift while traversing through the base-emitter junctions of $\mathrm{Q}_{\mathrm{in}}$ and $\mathrm{Q}_{\mathrm{d}}$, respectively. Switched Emitter Follower (SEF) consisting of $\mathrm{Q}_{\mathrm{s} 1}$, $\mathrm{Q}_{\mathrm{s} 2}$, and $\mathrm{Q}_{\text {out }}$ is adopted as the switch element of the THA due to its superior speed and linearity. Moreover, by employing a constant bias current, SEF does not contribute a signal-dependent charge injection. The value of this bias current is chosen such that the third harmonic component $\mathrm{HD}_{3}$ of the signal at the output of the SEF is bounded to -75 dB at the Nyquist frequency of 500 MHz .
The boost in track-mode linearity is created by injecting an assisting current provided by the auxiliary SEF into the hold capacitor $\mathrm{C}_{\mathrm{h}}$ through the feedforward capacitor $\mathrm{C}_{\mathrm{ff}}$. Note that $\mathrm{C}_{\mathrm{ff}}$ and $\mathrm{C}_{\mathrm{h}}$ sustain the same signal excursion, therefore, the current of $\mathrm{C}_{\mathrm{ff}}$ is reused to provide that of the hold capacitor $\mathrm{C}_{\mathrm{h}}$ in the track mode. This significantly reduces the $V_{\mathrm{BE}}$ modulation in $\mathrm{Q}_{\text {out }}$ so that the THA attains the track mode linearity of 9.4 b at Nyquist frequency of $500 \mathrm{MHz} . \mathrm{Q}_{\text {clp }}$ clamps the voltage of node A in Fig. 2 to a replica of the held signal during the hold mode. This prevents the voltage of node A from falling to an unknown value during hold mode, which otherwise would hinder the turn-on of $\mathrm{Q}_{\text {out }}$ during hold-to-track transition. As perceived in the schematic of Fig. 2, $\mathrm{Q}_{\mathrm{d}}$ is turned off during the hold mode and $\mathrm{Q}_{\mathrm{clp}}$ controls


Fig. 2: THA, half cell.
the voltage of node A. The replica of the held signal, stored across $\mathrm{C}_{\mathrm{ff}}$, is shifted up by PMOS transistor $\mathrm{M}_{\mathrm{sh}}$ to alleviate the down-shift it experiences while traversing through the base-emitter junction of $\mathrm{Q}_{\mathrm{clp}}$. The value of the up-shift is slightly larger than one $V_{\mathrm{BE}}$. Therefore, node A is clamped to a voltage which is slightly larger than the held value, faintly forward biasing $\mathrm{Q}_{\text {out }}$ during the hold mode. This expedites the turn-on of $Q_{\text {out }}$ during hold-to-track transition, preventing $\mathrm{C}_{\mathrm{h}}$ from being discharged by $\mathrm{Q}_{\mathrm{s} 2}$. Crossed feedback capacitors $\mathrm{C}_{\mathrm{fb}}$ are devised to further improve the hold mode feedthrough and equalize the commonmode levels at the outputs of THA. These techniques enable the THA to maintain a linearity of 10.9 b at low frequencies, with a negligible drop, to 10.5 b at the Nyquist frequency of 500 MHz .

Shown in Fig. 3, a fully differential reference ladder obviates the need for dc references and eliminates "reference bowing" due to the input bias current of the following array of emitter followers. In the differential reference ladder, the INL requirement sets a lower limit on the number of the taps for a given spread in tap resistance as demonstrated in (1):

$$
\begin{equation*}
I N L_{\max }=2^{n-1} \frac{\sqrt{N-1}}{N} \sigma_{\delta R / R} \tag{1}
\end{equation*}
$$

where n is the ADC resolution, N is the number of the taps, and $\sigma_{\delta R / R}$ denotes the spread in the tap resistance (less than $1 \%$ ). On the other hand, the distributed nature of the loading places an upper limit on the number of stages that reference ladder can drive. Here, 40 zero-crossings ( 32 in-range) are tapped from the reference ladder to bound the INL to less than 1LSB. This results in an excessive propagation delay through the reference ladder which is compensated by pipelining the analog core. Padding 4 out-of-range zero-crossings (dummies) on each side of the full scale guarantees that the folding amplifiers exhibit a nonclipping folded characteristics across the entire range of input. This is of crucial importance to the


Fig. 3: Differential reference ladder.
accuracy of the interpolating and averaging operations at the boundaries of the input range. The ratio of tap voltage ( $V_{\text {Tap }}$ ) to thermal voltage ( $V_{\mathrm{TH}}$ ) determines the INL peak due to interpolation between the hyperbolic tangent transfer characteristics of the emitter-coupled pairs. The current design adopts a tap voltage of 25 mV to confine the INL peak to less than 0.5 LSB . This results in an LSB voltage of $V_{\text {LSB }}=$ $\left(2 \times V_{\text {Tap }}\right) / I F=1.5625 \mathrm{mV}$ where IF is the aggregate interpolation factor of 32 . The resulting LSB voltage is large enough to combat the random offset voltage of the comparators ( $1 \sigma=2.7 \mathrm{mV}$ ) with a moderate aggregate quantizer gain of $A_{\mathrm{v}}=5.2$. This also leads to a differential full scale input voltage of $2^{10} \times V_{\text {LSB }}=$ $1.6 \mathrm{~V}_{\mathrm{p}-\mathrm{p}}$.

The folding degrees of 5 and 8 are implemented in the first and second folder, respectively. This choice of the folding degrees optimizes the total power consumption of the analog core by incorporating only 32 and 11 comparators in the fine and coarse quantizers. Shown in Fig. 4, the first folder comprises of five emitter-coupled pairs whose outputs are connected in alternating fashion to two identical load resistors, and whose inputs are connected to appropriately defined reference voltage levels. The INL peak resulting from the mismatches of the tail currents in $5 \times$ folder can be derived as follows:

$$
\begin{equation*}
I N L_{\max }=I F\left(\frac{V_{T H}}{V_{T a p}}\right) \sqrt{F F_{1}-1} \sigma_{\delta I / I} \tag{2}
\end{equation*}
$$

where $F F_{1}$ is the folding degree of 5 and $\sigma_{\delta I / I}$ is the spread in the tail current sources of the $5 \times$ folder which is less than $1 \%$ attained through the superior matching of the degenerated BJT current sources. Equation (2) yields a peak INL of 0.8 LSB which is alleviated to less than 0.5 LSB through averaging property of the resistive interpolation networks.

Since the second folder has an even degree (8) with folded signals as inputs, the architecture of Fig. 4 for the second folder would result in a highly distorted


Fig. 4: $5 \times$ folder.
folded signal which is not useful. Therefore, the folding degree of 8 is realized via cascading three stages of Gilbert-type multipliers [6], illustrated in Fig. 5. The inputs of the multiplier (at ports A and B) must hold a phase shift of $90^{\circ}$ in order that the zerocrossings of the product signal are equally spaced. This design exploits this $90^{\circ}$ phase shift to operate the emitter-coupled pairs in the multipliers on the verge of the clipping. The resulting benefit is twofold. First, at the vicinity of the zero-crossings, the linearity of the multiplier output is improved since one of the pairs and, hence, its associated nonlinearity, captured by the tanh function, is decommissioned. Second, as one pair is nearly clipped (constant amplitude), the amplitude variations at the multiplier output due to the $V_{\mathrm{BE}}$ mismatches between the transistors in the nonclipped pair are minimized. This improves the integral linearity at the zero-crossings generated by the $8 \times$ interpolator following the multiplier trees so that the ADC achieves the record peak SNDR of 55.6 dB . As seen in Fig. 1, the differential reference ladder combined with $3 \times$ folders, $4 \times$ interpolator, and $8 \times$ folders also provide the coarse encoder with "windows", each comprising of two phase-shifted folded signals. The coarse encoder utilizes these windows to extract the most significant bits $\left(b_{0} b_{1} b_{2}\right.$ $b_{3}$ ) synchronized with the least significant bits ( $b_{4} b_{5}$ $b_{6} b_{7} b_{8} b_{9}$ ) with the aid of bit-sync $b_{4}$, as illustrated in Fig. 1. The phase shift span in the windows determines the maximum offset between the fine and coarse comparators that can be tolerated. The choices of folding degrees and first interpolation factor result in a $32 V_{\text {LSB }}$ offset tolerance between the fine and coarse quantizers which is significantly larger than $1 \sigma$ offset of 2.7 mV in the comparators.

When THA enters the hold phase, settling transients at the output of the first folder creates excessive dynamics at the output of the second folder due to its frequency multiplication property. Exacerbated by the loading of the RC network formed by the $8 \times$ interpolation and the input capacitance of the fine comparators, settling time at the output of the second folder becomes prohibitive to attain the conversion speed of $1 \mathrm{GS} / \mathrm{s}$. To surpass the settling burden, this design employs pipelining principle [7], by


Fig. 5: Gilbert-type multiplier cell.
incorporating distributed THAs after each folder. This creates an extra 1 ns window for the signal transients at the input of the fine comparators to subside so that the signal polarity is correctly detected. The distributed THAs are a simplified version of the front-end THA with a significantly lower power dissipation of 12 mW . Interstage distributed THAs also disturb the timing relations among windows derived from the intermediate stages of the analog core assisting the coarse encoder. Therefore, a "Window Synchronizer", shown in Fig. 1, is realized to synchronize these windows with bit-sync $b_{4}$.

Considering the amplified LSB voltage of $\approx 8 \mathrm{mV}$ at the comparators input, the comparator must achieve a total input referred offset voltage with $1 \sigma \leq 2.7 \mathrm{mV}$ at 1 GHz conversion rate so that $3 \sigma \leq 8 \mathrm{mV}$. A full CMOS design leads to excessive capacitive loading on the $8 \times$ interpolation network and offset, prohibiting its use in this architecture. To avoid excessive capacitive loading on the $8 \times$ interpolation network while providing a rail-to-rail swing, a two stage solution is proposed as demonstrated in Fig. 6.


Fig. 6: The first stage bipolar and the second stage CMOS comparator.

An on-chip clock generator is designed to shift the phase of the master clock in eight steps (each 125 ps ). This is devised to ensure that, under random process variations, pipeline stages sampling occurs after the dynamics of their inputs have subsided.

## IV. EXPERIMENT RESULTS

The ADC is implemented in a $0.35 \mu \mathrm{~m}$, four-metal, single-poly SiGe BiCMOS process with a transistor $f_{t}$ of 60 GHz . The micrograph of the chip is shown in Fig. 7. It occupies an active area of $4.5 \times 1.2 \mathrm{~mm}^{2}$ and consumes 2 W of power.


Fig. 7. Chip micrograph.
SNDR and SFDR at 1 GHz conversion rate with various input frequencies are plotted in Fig. 8. The SNDR is 8.9 ENOB at low input frequencies. This is the highest ENOB compared to any ADC with similar accuracy and speed to our knowledge. At 100 MHZ input frequency, SNDR is 8.3 ENOB and it eventually rolls off to 6.5 ENOB at the Nyquist frequency. The ADC exhibits 64 dB SFDR at 5 MHz while for a 100 MHz input the SFDR measures 60 dB . Insufficient linearity of the output buffer of distributed THAs and sampling aperture jitter ( 1.24 ps ) contributed mainly toward the SNDR degradation. Fig. 9 demonstrates the output spectrum for 5.00488 MHz sinusoidal input $\left(1.6 \mathrm{~V}_{\mathrm{p}-\mathrm{p}}\right)$ quantized at $1 \mathrm{GS} / \mathrm{s}$. The DNL and INL peak at the sampling rate of $1 \mathrm{GS} / \mathrm{s}$ are measured 0.4 LSB and 1.1 LSB , respectively. The DNL and INL profile are also depicted in Fig. 10. This ADC achieves the latency of one clock cycle in the analog core, surpassing those reported in [2]-[3] and [1] with twelve and four cycles of latency, respectively. Table 1 summarizes the performance metrics at $1 \mathrm{GS} / \mathrm{s}$ conversion rate and 5 MHz and 100.46 MHz input


Fig. 8: Measured SNDR/SFDR. Fig. 9: Output spectrum.


Fig. 10: INL/DNL.
TABLE I
PERFORMANCE SUMMARY

|  | $f_{\text {in }}=5 \mathrm{MHz}$ | $f_{\text {in }}=100.46 \mathrm{MHz}$ |
| :---: | :---: | :---: |
| Sample Rate, $f_{\mathrm{s}}$ | $1 \mathrm{GSample} / \mathrm{s}$ |  |
| Resolution | 10 bits |  |
| Latency | 1 Clock Cycle |  |
| Max INL | 1.1 LSB | 1.2 LSB |
| Max DNL | 0.41 LSB | 0.45 LSB |
| SNDR | 55.6 dB | 51.6 dB |
| SFDR | 64.1 dB | 59.8 dB |
| THD | $-60.7 \mathrm{~dB}$ | $-56 \mathrm{~dB}$ |
| ENOB | 8.9 | 8.3 |
| Aperture Jitter | $1.24 \mathrm{ps} @ f_{\mathrm{s}}=1 \mathrm{GS} / \mathrm{s} \& \mathrm{f}_{\mathrm{in}}=200 \mathrm{MHz}$ |  |
| ERBW | 100 MHz |  |
| Input Range | 1.6 V differential |  |
| Input Termination | $50 \Omega$ (100 $\Omega$ differential) |  |
| Supplies | 5.5 V (THA) and 3.5 V (ADC) |  |
| THA Current | 64 mA |  |
| Analog Core Current | 354 mA |  |
| Digital Current | 139 mA |  |
| L VDS Output Drivers | 140 mA |  |
| ADC Area | $5.3 \mathrm{~mm}^{2}$ |  |
| Dic Arca | $25 \mathrm{~mm}^{2}$ |  |
| Technology | 0.35 m BiCMOS (1-poly, 4-metal) |  |

frequencies. As seen in this table, the logic circuits and clock buffers consume one forth of the power while the analog core uses $60 \%$ of the total power. Using a more advanced BiCMOS process with higher transistor $f_{t}$ enables a lower power consumption.

## References

[1] S. Gupta, M. Choi, M. Inerfield, and J. Wang, "A 1GS/s 11 b Time-Interleaved ADC in $0.13 \mu \mathrm{~m}$ CMOS," ISSCC Dig. Tech. Papers, pp. 576-577, Feb., 2006.
[2] S. Louwsma, E. van Tujil, M. Vertregt, and B. Nauta, "A1.35 GS/s, 10b, 175 mW Time-Interleaved AD Converter in $0.13 \mu \mathrm{~m}$ CMOS," Symp. VLSI Circuits, pp. 62-63, June, 2007.
[3] C. Hsu, et al., "An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration," ISSCC Dig. Tech. Papers, pp. 464-465, Feb., 2007.
[4] K. Poulton, et al., "A 20GS/s 8b ADC with a 1 MB Memory in $0.18 \mu \mathrm{~m}$ CMOS," ISSCC Dig. Tech. Papers, pp. 318-319, Feb., 2003.
[5] A. Razzaghi, M. C. F. Chang, "A 10-b, 1-GSample/s track-and-hold amplifier using SiGe BiCMOS technology," in CICC Dig. Tech. Papers, Sept. 2003, pp. 433-436.
[6] P. Vorenkamp, R. Roovers, "A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC," IEEE J. Solid-State Circuits, vol. 32, no. 12, pp. 1876-1886, Dec., 1997.
[7] M. Choe, B. Song, K. Bacrania, "An 8-b 100MSample/s CMOS Pipelined Folding ADC," IEEE J. Solid-State Circuits, vol. 36, no. 2, pp. 184-194, Feb., 2001.

