An Energy-Efficient and High-Speed Mobile Memory I/O Interface Using Simultaneous Bi-Directional Dual (Base+RF)-Band Signaling

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Abstract—A fully-integrated 8.4 Gb/s 2.5 pJ/b mobile memory I/O transceiver using simultaneous bidirectionaldual band signaling is presented. Incorporating both RF-band and baseband transceiver designs, this prototype demonstrates an energy-efficient and high-bandwidth solution for future mobile memory I/O interface. The proposed amplitude shift keying (ASK) modulator/demodulator with on-chip band-selective transformer obviates a power hungry pre-emphasis and equalization circuitry, revealing a low-power, compact and standard mobile memory-compatible solution. Designed and fabricated in 65-nm CMOS technology, each RF-band and baseband transceiver consumes 10.5 mW and 11 mW and occupies 0.08 mm² and 0.06 mm² die area, respectively. The dual-band transceiver achieves error-free operation (BER <10⁻¹⁵) with 2²³-1 PRBS at 8.4 Gb/s over a distance of 10 cm.

Index Terms—Amplitude-shift-keying (ASK), dual-band signaling, impedance transformation, mobile memory interface, multi-band RF-Interconnect (RF-I), simultaneous bidirectional.

I. INTRODUCTION

S MOBILE devices (such as smart phones) continue to enhance video processing and graphics-intensive computing capabilities, they keep demanding greater aggregate memory bandwidths, projected to reach 12.8 GB/s in the near future [1]. However, battery energy efficiency, fast power mode transition timing, and thermal dissipation constraints are expected to impose more strict challenges for improving both energy efficiency and aggregate data throughput. Current DDR memory I/Os operate at 5 Gb/s with a power efficiency of 17.4 mW/Gb/s (i.e., 17.4 pJ/b) [2], and graphic DRAM I/Os

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operate at 7 Gb/s/pin [3] with a power efficiency worse than that of DDR. Therefore, future mobile memory I/O interfaces will require both much higher bandwidths and better power efficiency.

Recent research [4]–[6] has led to the demonstration of unidirectional serial links using low-swing differential signaling with terminated channels, sensitive offset calibrated receivers and voltage mode line drivers with excellent power efficiency (i.e., $\sim 1 \text{ mW/Gb/s}$ [7]) compared to that of current mobile memory interfaces. However, these links are unsuitable for mobile memory I/O interfaces for the following reasons: 1) using symmetric links between two similar devices, as opposed to the master/slave configuration in a memory interface, and 2) requiring extensive initialization time [1] (~ 1000 clock cycles [1]), which becomes problematic to meet mobile DRAM I/O needs in switching between active, stand-by, self-refresh and power-down operation modes [1]. Simultaneous bidirectional (SBD) interconnect [9]-[11], has also been developed to facilitate increased aggregate memory bandwidth with simultaneous and bidirectional point-to-point communication links. However, such interconnect encounters challenges from reduced input signal noise margin due to increased number of voltage references and higher crosstalk and inter-symbol interference (ISI) due to the low-pass effects of the channel [11], which in either case degrades its bit-error rate (BER).

Furthermore, traditional baseband-only (or BB-only) signaling [2], [3], [15] also tends to consume power super-linearly with extended bandwidth [1], partially due to the needs of power hungry pre-emphasis, and/or equalization circuitry. To overcome such technical obstacles, we hereby present the use of a dual-band interconnect (DBI) [8], [17] to enable a simultaneous bidirectional memory I/O interface with both high throughput data rate and low-power circuit operation. Compared to the conventional BB-only signaling, the proposed DBI, as shown in Fig. 1 uses both baseband and RF-bands for simultaneous and bidirectional dual-data-stream communication through a shared transmission line (T-Line). This dual (BB+RF) band concept can be further extended to Base + Multiple-RF bands in the future. Instead of limiting the baseband-only interconnect operation within its linear-power-consumption region versus the bandwidth, we can double the interface bandwidth by using the DBI and still maintain in the linear power-consumption versus the bandwidth region in each of the two bands.

Controller Memory D1(RF) IN D1(RF) OUT D1(RF) 11010 11010 **∮** Diff. DQ x N D2(BB) OUT D2(BB) IN 01011 01011 D2(BB) 6 Þ **DBI** chip CII DLL (or PLL Diff. CLK (a) **Proposed Dual Band Signaling** RFband Baseband-only Baseband Signal Signal Signal Signal Signal Power Power f(RF) f(BB) f(BB) (b)

Fig. 1. (a) DBI-based mobile memory interface architecture with forward-clock for simultaneous bidirectional signaling. (b) Dual-band signaling in frequency domain.

Moreover, with simple forwarded clocking that adds a small overhead to mobile DRAM I/O, the DBI can facilitate an SBD data link as well. By applying such links to DRAM I/O data (DQ) and command/address (C/A), we can greatly reduce the DRAM access time by requesting DRAM read/write operations concurrently. In summary, by using the DBI, we can implement the SBD DRAM I/O interface with a much higher aggregate data rate (up to 8.4 Gb/s and 10 Gb/s at standard FR4 and Rogers 4003 [13] test boards, respectively), and a low-power operation (<2.5 mW/Gb/s) to meet the mobile memory I/O requirements [1].

The remainder of this paper is organized as follows. Section II describes the DBI transceiver architecture and discusses its advantages and considerations. Section III covers the design details of a DBI transceiver, signal integrity, and channel modeling. Measurement results are given in Section IV. Our conclusion is presented in Section V, followed by an analysis of impedance-matching for a transformer-based receiver in the Appendix.

II. DBI INTERFACE ARCHITECTURE

Fig. 1(a) shows the proposed DBI-based mobile memory interface architecture where the DRAM device can operate directly from a forwarded clock from the memory controller, without a PLL/DLL, to synchronize the entire interface. Fig. 1(b) shows the intended DBI signaling that contains both base and RF-bands for simultaneous communications.

The proposed dual-band interconnect (DBI) system architecture contains a set of baseband transceiver (BBTX, BBRX) and a set of RF-band transceiver (RFTX, RFRX) with shared offchip differential transmission line. In this system, when BBTX and BBRX communicate with each other by using a commonmode signaling at the baseband, the RFTX and RFRX communicate concurrently by using a differential-mode signaling at the 23 GHz RF band. The proposed dual (RF + base) band signaling is aimed to twice the data rate through two different frequency bands without any latency penalty. Fig. 1(b) shows the dual band frequency allocations for two concurrent I/O channels. The key challenge in designing this dual-band interconnect system is to reduce the RF-band transceiver's area and power overhead, while achieving a sufficient spectral isolation between two communication bands. These technical challenges are overcome by using forward clocking and ASK (de)-modulation schemes. The forward clocking scheme on the DRAM side can reduce the clock overhead of DRAM, support faster power switching modes [1], and synchronize skews between dual data channels on the DRAM side with no need of power hungry clock and data recovery (CDR) and phase synchronization circuitry [8]. The memory controller forwards a half bit-rate clock to the DRAM over the clock line (CLK). The forwarded clock is directly buffered to time the DRAM transmit and receive circuits. This eliminates the need for any PLL or DLL on the DRAM, with all phase compensation performed by the memory controller side, allowing fast DRAM power mode transitions and resulting in a simplified DRAM clock architecture.

III. TRANSCEIVER CIRCUIT DESIGN

A. Baseband Transceiver (BBTX, BBRX)

Fig. 2(a) shows the baseband transmitter (BBTX) which utilizes a low common-mode push-pull output driver with two resistors in a series with transistors. To avoid impedance mismatch and reduce sensitivity to process, voltage and temperature (PVT) variations, the BBTX has a digitally controlled off-chip



Fig. 2. (a) Baseband transmitter with digitally controlled OCD impedance logic. (b) Simulated OCD resistance versus control code.

driver (OCD) impedance circuit. The OCD is composed of multiple binary-weighted sub-drivers and decoder logics to provide digitally controllable driver strength by selectively enabling the sub-drivers [12]. The strength of the OCD simulated as a function of the digital control code is shown in Fig. 2(b). Regardless of the PVT variations, there are sufficient control codes to control the OCD strength with the value of 50 $\Omega \pm 15 \Omega$ matching the required resistance to the impedance of off-chip T-Line (singled-ended perspective).

Fig. 3(a) shows the baseband receiver (BBRX) which amplifies the incoming data stream D2 (BB) using buffers with a digitally controlled on-die termination (ODT) to set the commonmode voltage (VTERM) and remove the impedance mismatch for optimal signal integrity [12]. The ODT should be switchable so that it controls resistance for the baseband receiver matching capability. The ODT is implemented with the series connection of a passive resistor and a transistor, as shown in Fig. 3(a). The required resistance value of the ODT should be 50 Ω which is same as the impedance of T-Line. To avoid the process variation of on-chip passive resistor (typically +/-20%), the ODT value can be controlled from 60 Ω to 40 Ω on the DBI link. The simulated worst case (impedance mismatched versus matched) waveforms are shown in Fig. 3(b). In summary, the strength of the OCD is calibrated to obtain accurate driver strength and the baseband data link is terminated by ODT resistors regardless of process variation.



Fig. 3. (a) Baseband receiver with digitally controlled ODT impedance logic. (b) Simulated BBTX output waveform.

B. RF-Band Transceiver (RFTX, RFRX)

Fig. 4 shows the RF-band transmitter (RFTX) which contains an LC tank VCO, an ASK modulator and a band-selective transformer. In RFTX, the VCO first generates RF carrier at 23 GHz and continuously modulates M1 and M2 for ASK communication. The data stream D1 (RF) modulates the 23 GHz carrier by switching on/off the current flow through M3 and M4 to complete the ASK modulation. The modulated output is then inductively coupled into an off-chip T-Line by way of an on-chip differential transformer. The simulated waveforms of the D1 (RF) input and ASK modulated output are shown in Fig. 4.

Fig. 5 shows the RF-band receiver (RFRX) which consists of a transformer and demodulator. For energy-efficient and compact design, the proposed RF demodulator uses non-coherent direct down-conversion scheme. Since a non-coherent detector only senses the envelope of an incoming signal, the proposed receiver does not require the power-hungry phase and frequency synchronizer. The RFRX first rejects the BB data stream by using an on-chip frequency-selective transformer. The bandpass filtered RF-band data stream is then injected into the receiver differential mutual-mixer which is composed of a selfmixer [16] and resistor-feedback amplifier and down-converted to the baseband data D1 (RF). In addition to the band-pass filter capability, the on-chip transformer acts as impedance matching device as well as passive amplifier for the incoming RF band



Fig. 4. (a) RF-band transmitter by using ASK modulation. (b) Simulated RFTX waveforms.

signal. A more detailed analysis on transformer design will be given in the following section. At the mutual mixer, the termination voltage and the tail current source determine the operating point, and the bootstrapped signal is extracted at the output node. We utilize a class-AB amplifier with resistive feedback to cancel offset and further filter out the residue of the RF carrier. The simulated incoming ASK modulated signal, differential mixer output, and recovered baseband data are summarized in Fig. 5.

Fig. 6 shows a DBI working mechanism for SBD dual data communication on a channel. Both of the 2-D MOMENTUM and 3-D HFSS simulations for transformer design and ADS circuit simulation [14] have been performed on the complete DBI architecture as a part of the design cycle. From baseband signaling perspective, the signal is fed into the center tap of the primary coil and transferred to the channel in common-mode. On the receiving end, the baseband signal is extracted through the center tap of a secondary coil. In the case of RF-band signaling, the differential signal is injected into the differential port of a primary coil and then coupled to the channel through a secondary coil.

C. Transformer Design for Impedance Matching and Band-Pass Filtering

In this prototype design, an on-chip transformer with primary-to-secondary-coil turn ratio of 1:2 is chosen to accomplish the needed signal gain, impedance matching, band-passfiltering and output power transfer. Unlike the baseband signaling, the RF-band signal cannot be terminated by using a simple resistor, since the parasitic around the resistor would dominate at high frequencies. Consequently, the proposed RF transceiver uses on-chip transformers as matching devices with simplified network illustrated in Fig. 7(a). The transformer is loaded by the mutual-mixer input stage with impedance modeled by series connection between a resistor and a capacitor. The detailed step-by-step analysis is given in the Appendix. Looking into the secondary coil of the transformer, an RLC resonant tank is formed with the impedance shown as the dashed line in Fig. 7(b). The real part of the mutual mixer input impedance (modeled as R in Fig. 7(b)) is boosted to roughly 200 Ω due to the intended resonance at the carrier frequency of 23 GHz, which corresponds to an impedance of 50 Ω at the transformer input side (primary coil) shown as a solid line in Fig. 7(b). In Fig. 7(c), we plot the input reflection coefficient (S11) of both the physical transformer (dashed line) and its equivalent lumped RLC model (solid line) to confirm our analysis on the



Fig. 5. RF-band receiver with band-selective on-chip transformer and simulated RFRX waveforms.

impedance matching. In both cases, S11 confirms the input reflected power below -30 dB near the self-resonant frequency.

The transformer also rejects the unwanted frequency band of signals, which is the transmitted baseband signal in this case. Looking from the controller side, the transmitted power does show a band-pass characteristic, and the rejection of the baseband is more than 20 dB, as indicated in Fig. 7(d) (assuming that the baseband spectrum occupies up to $2.5 \sim 3$ GHz). The transmitted power is about 6 dB higher at the secondary coil of the transformer again due to the 1:2 transformer turn ratio. In summary, the impedance matching and the rejection of unwanted frequency band can be effectively achieved by utilizing the on-chip transformer.

D. DBI Memory Channel Modeling, Signal Integrity and Latency

It is important to analyze the frequency characteristic of the memory channel on FR-4 PCB, since the RF-band signal may

suffer from significant loss in the carrier frequency of 20 GHz. For an accurate channel modeling including wire bonds and parasitic capacitance, the 3-D EM solver tool (HFSS) is used to generate S parameters. The simulated signal loss of the 10 cm FR-4 PCB T-Line (Fig. 8(b)) is -8.9 dB at 23 GHz as shown in Fig. 8(c). The loss will be substantially reduced provided the memory interface distance is much shorter than 10 cm (typically $\sim 1-2$ cm) in modern mobile devices.

Currently, the DDR-SDRAM's high-speed parallel link reaches its physical limit originated from channel crosstalk and supply noise [2]. The channel crosstalk especially takes a dominant portion of the over 7 Gb/s timing budget, becoming the main barrier for further speed improvement [2]. In order to evaluate DBI crosstalk effects, multiple DBI channels are modeled by considering the electromagnetic coupling from adjacent channels as shown in Fig. 9(a). There are two possible cases. The first is an optimistic case where one DBI channel is idle and the other is working. The second is an extreme



Fig. 6. DBI working mechanism for simultaneous bidirectional dual data transaction.

crosstalk case where both DBI channels are working concurrently. Fig. 9 shows eye-diagrams of BB and RF-band with and without crosstalk at single and multiple lanes. The crosstalk occurs whenever the electromagnetic fields from multiple channels interact. This phenomena cause crosstalk-induced timing distortion since the propagation time of a T-line varies depending on the transition of adjacent channel [2]. The worst simulated crosstalk-induced timing distortion is 21 ps (BB) and 49 ps (RF-band), respectively, because large swing base band signal impacts on small swing RF-band signal at multiple DBI channels. In either case, reliable DBI communications can be established.

Typical memory channel has 8 or 16 lanes. To extend one lane to multiple lanes per clock, the total timing distortion of BB and RF-band should be small enough so that the DBI transceiver of the DRAM side can sample dual-band data based on a forwarded reference clock from the MCU (BBTX). Total timing distortion is composed of static latency difference between BB and RF-band, crosstalk from multiple data lanes and latency mismatches of DBI transceiver. Fig. 10 shows the simulated latency of DBI transceiver and total timing distortion considering crosstalk (29 ps (BB) and 49 ps (RF-band)) and latency mismatches (i.e., 5.6 ps = 1.87 ps $\times 3$ @ 3 sigma of RF-band). The crosstalk from multiple channels is a key portion of total timing distortion. When the total timing distortion on the DRAM side is less than half clock cycle (i.e., 250 ps @ 2 GHz = 4 Gb/s data rate), the forward clocking scheme can synchronize skews between dual data channels on the DRAM side without DLL/PLL and CDR. It is assumed that the timing skew of ($8 \times$ DQ) clock distribution at the DRAM side may be tracked by a delay compensation scheme.

The VCO startup time may cause latency penalty for simultaneous bidirectional communication because RF-band transceiver uses 23 GHz VCO. To mitigate this possible latency overhead of RF-band transceiver, an additional VCO startup control logic may be needed as shown in Fig. 11. When the CS (Chip Select) control signal asserts, a VCO startup control signal turns on a VCO ahead of two clock cycles of data strobe (DQS) signal. After CS signal deasserts, the VCO control logic turns off the frequency generation VCO circuit to save power.



Fig. 7. (a) Transformer design and model. (b) Input impedance at each point. (c) Input reflection coefficient S11. (d) Transmitted power at each point.



Fig. 8. (a) DBI memory channel modeling with wire-bonding. (b) FR-4 test board. (c) Simulated signal loss of FR-4 channel.



Fig. 9. Signal integrity simulation (a) Test setup of single/multiple channel and HFSS model of multiple channels. (b) Simulated data eye-diagram with and without crosstalk at single/multiple channels.

IV. MEASUREMENT

The DBI transceiver has been designed and fabricated in 65 nm CMOS technology to demonstrate dual-band bidirectional communication on a shared PCB T-Line. The base and RF-band transceivers consume 11 mW and 10.5 mW respectively from a single 1.0 V supply. Fig. 12 shows the die photo of a DBI transceiver, where the base and RF-band transceivers occupy 0.056 mm² and 0.084 mm² (with on-chip transformers) respectively. Two designs are integrated for either a controller or DRAM side so that two devices can implement the complete

interface architecture shown in Fig. 1. The 23 GHz VCO which seems difficult to be implemented in poor DRAM process is placed at the memory controller side which typically uses a CMOS process as the DBI experiment as shown Fig. 12. The BBTX which operates at the speed of 2.5 GHz @5 Gb/s and RFRX which is only composed of passive element and active differential mutual mixer exist at the DRAM side in order to be better feasible in DRAM process.

To verify the signal integrity, we also conducted a complete BER test. Fig. 13 shows the demonstration setup for a DBI communication and BER measurements. It is necessary



Fig. 10. Simulated latency of DBI transceiver and total timing distortion considering crosstalk from multiple channels and latency mismatches.

to measure the frequency spectrum characteristic of carrier generator to demonstrate a dual-band communication. The spectrum testing setup and frequency spectrum of the RF carrier at 23 GHz are depicted in Fig. 14. Note that RF carrier measurements (-54 dBm) is conducted under the significant signal loss through cable, connector and the GSG probe, which is not de-embedded and calibrated.

Fig. 15 shows the measured waveforms for DBI input and recovered data streams. Fig. 16 shows measured eye diagrams of aggregate 8.4 Gb/s (4.6 Gb/s BB + 3.8 Gb/s RF-band) data throughput over a 10 cm T-Line on a FR-4 board and 10 Gb/s (5 Gb/s BB + 5 Gb/s RF-band) over the same distance T-Line on a Rogers 4003 board, respectively. The measured eye diagrams are taken from the output driver. These eye diagrams demonstrate that good signal integrity can be achieved at these data rates with the proposed dual band signaling. Table I shows the performance comparison to the prior arts. The conventional interface [1], [2], [15] utilize only baseband signaling. Compared to the latest mobile memory interface using differential signaling [1], the DBI can double the data rate with 25% less power consumption.

V. CONCLUSION

We designed and fabricated a DBI for a mobile DRAM I/O interface in 65 nm CMOS to obtain an aggregate data throughput of 8.4 Gb/s and 10 Gb/s on FR-4 and Rogers 4003 test boards, respectively, with a power consumptions of 21 and 25 mW. The BERs for both test boards are measured as $< 1 \times 10^{-15}$ by using 2^{23} –1 PRBS. The proposed DBI interface is able to meet the highest aggregate data throughput and best energy efficiency demands of future mobile memory I/O link system in conventional cost-effective packaging technology with the smallest active die area.

Appendix Analysis of Impedance Matching for a Transformer-Based Receiver

The input impedance of a transformer is referred to as a *reflected impedance*, meaning that the input impedance is reflected from the load impedance. The main purpose of this Appendix is to understand how the impedance transformation behaves at the input terminal of the transformer.



Fig. 11. Timing diagram of VCO startup control logic and simulated VCO startup delay.



Fig. 12. (a) Die photo of DBI transceiver.

As shown in Fig. 17, it is clear that the input impedance of a mutual mixer consists of frequency-dependent resistance and capacitive reactance, which can be approximated using the following equation within the bandwidth of interest:

$$Z_{mix}(\omega) = Z_{mix,R}(\omega) - jZ_{mix,I}(\omega)$$
 (A.1)

where Z_{mix} is the total input impedance of mutual mixer $Z_{mix,R}$ and $Z_{mix,I}$ and are the real and imaginary part, respectively. As shown in Fig. 17(a), $Z_{mix,R}$ (dashed line) is almost constant and $Z_{mix,I}$ (circled line) increases linearly, which means the input impedance of mutual mixer can be modeled as series connection of resistor and capacitor. Then the simplified input impedance network can be modeled with inductance (L) of the secondary spiral of transformer and resistance ($R_S = 2\pi f_r L/Q$, where f_r and Q is the self-resonant frequency and quality factor of the secondary spiral of transformer, respectively). Instead of analyzing complicated transformer network, we choose to understand the resonant effect of secondary coil first. The equivalent input impedance of secondary coil can be calculated as follows:





Fig. 13. Demonstration of DBI communication and BER measurement setup.

$$Z_{2in}(s) = (sL + R_s) \| (R + 1/sC)$$

= $R \frac{s^2 + \left(\frac{R_s}{L} + \frac{1}{RC}\right)s + \frac{R_s}{R}\frac{1}{LC}}{s^2 + \frac{(R_s + R)}{L}s + \frac{1}{LC}}$. (A.2)

The main interest of equation (2) is to find the impedance value at the resonant frequency. Before further analysis, since there are two zeros and two poles, the (A.2) needs to be confirmed that it is indeed band-pass characteristic based on R, L,



Fig. 14. (a) Tone test setup. (b) Measured 23 GHz RF-band carrier on DBI channel.



Fig. 15. Measured simultaneous bidirectional 8.4 Gb/s Dual (Base+RF)-band waveform.



Fig. 16. Measured eye diagrams of aggregate 8.4 Gb/s (4.6 Gb/s BB + 3.8 Gb/s RF-band) and 10 Gb/s (5 Gb/s BB + 5 Gb/s RF-band) data rate, respectively, on FR-4 and Rogers 4003 test boards.

and C values. For example, from Fig. 15(a), the imaginary part of impedance is around -55Ω , and total load capacitance and required inductance of secondary coil can be calculated using

$$C = \frac{1}{2\pi f_r Z_{2in,I}(f_r)} \tag{A.3}$$

$$L = \frac{1}{(2\pi f_r)^2 C} \tag{A.4}$$

Based on (A.3) and (A.4), C is roughly 130 fF, L is 380 pH, R_S is 4 Ω (the simulated Q is 15 at $f_r = 23$ GHz), and Ris 12 Ω from Fig. 15(a). Based on the calculated values, the pole-zero map and its frequency response of input impedance network can be plotted. As shown in Fig. 17(c), zeros are negative real numbers and the imaginary part of pole is much larger than its real part, which shows the band-selective frequency response as shown in Fig. 17(d). For proper impedance matching, the key is to calculate input impedance value at its resonant frequency. From the denominator of (A.2) and the resonant frequency ($\omega = 1/\sqrt{LC}$) under the sinusoidal steady state condition, (A.2) becomes

$$Z_{2in}(j\omega) = R \frac{-\omega^2 + j\left(\frac{R_s}{L} + \frac{1}{RC}\right)\omega + \frac{R_s}{R}\frac{1}{LC}}{-\omega^2 + j\frac{(R_s + R)}{L}\omega + \frac{1}{LC}}.$$
 (A.5)

At the resonant frequency, the equation (5) becomes

$$Z_{2in} = R \frac{\left(\frac{R_s}{L} + \frac{1}{RC}\right) \frac{1}{\sqrt{LC}} + j\left(\frac{1}{LC} - \frac{R_s}{R} \frac{1}{LC}\right)}{\frac{(R_s + R)}{L} \frac{1}{\sqrt{LC}}}.$$
(A.6)

As the imaginary part of equation (6) goes to zero at the resonant frequency and the term $(R_s RC)$ is much smaller than L/C(~ on the order of 1000), the real part can become

$$Re(Z_{2in}) = \frac{RL\left(\frac{R_s}{L} + \frac{1}{RC}\right)}{(R_s + R)} = \frac{R_sRC + (L/C)}{R_s + R} \cong \frac{(L/C)}{R_s + R}.$$
(A.7)

Fig. 17(d) clearly shows that the equivalent impedance of secondary spiral can be transformed and boosted by the resonant effect of the transformer and the simulated impedance is 227 Ω at the resonant frequency with actual parasitic loadings of the proposed differential mutual mixer. Ultimately, the transformer turn ratio and coupling coefficient should be designed depending on the impedance value (Z_{2in}) of the secondary spiral to match the impedance (50 Ω single-ended wise) of an off-chip memory channel. Based on the transformer model shown in Fig. 17(b), the reflected impedance seen from the input of transformer can be calculated as

$$Z_{1in} = R_{s1} + j\omega L_1 + \frac{\omega^2 M^2}{R_{s2} + j\omega L_2 + Z_{2in}}$$
(A.8)

where R_{s1} , L_1 , R_{s2} and L_2 are series resistance and inductance of first and second spiral of transformer, respectively and M is mutual inductance. Equation (A.8) can be rearranged with the real and imaginary parts, where the real part can be interpreted



Fig. 17. (a) Simulated input impedance. (b) Lumped circuit to analyze input impedance Z_{in} . (c) Pole-zero map. (d) Simulated frequency response of input impedance.

 TABLE I

 COMPARISON WITH STATE-OF-THE-ARTS

	[2] JSSC	[15] ISSCC	[1] JSSC	This Work	
	2009	2009	2010	FR4 DBI	Roger DBI
Technology	0.18μm CMOS	0.13μm CMOS	40nm CMOS	65nm CMOS	65nm CMOS
Bands	BB	BB	BB	BB+RF(23GHz)	BB+RF(23GHz)
Supply	1.8V	1.2V	1.1V	1.0V	1.0V
T-Line Length	10cm (FR4)	5cm (N/A)	7cm (FR4)	10cm (FR4)	10cm (Roger)
Aggregate	(BB-only)	(BB-only)	(BB-only)	(RF+BB)	(RF+BB)
data rate	5Gb/s	6.0Gbps	4.3Gbps	8.4Gb/s	10Gb/s
Communication	Bidirectional	Bidirectional	Bidirectional	Simultaneous Bidirectional	Simultaneous Bidirectional
Energy per bit	17.4pJ/bit	15.8pJ/bit	3.3pJ/bit	2.5pJ/bit	2.5pJ/bit
Total power	87mW	95mW	14.4mW	11mW (BB) 10mW (RF)	13mW (BB) 12mW (RF)
Chip Area	0.52mm ²	0.30mm ²	N/A	0.14mm ²	0.14mm ²
Measured BER	10 ⁻¹² (PRBS2 ¹⁵ -1)	10 ⁻¹² (PRBS2 ¹⁵ -1)	N/A	<10 ⁻¹⁵ (PRBS2 ²³ -1)	<10 ⁻¹⁵ (PRBS2 ²³ -1)

as the reflected impedance from the secondary while the imaginary part is the reactive element from the primary spiral. Because the reflected impedance can be seen simply as a resistor at the resonant frequency of the secondary, the inductance of the primary can be evaluated by using (A.9):

$$L_{1} = \frac{50 \times L_{2} \left[\left(\frac{R_{L}}{2\pi f_{r} L_{2}} \right)^{2} + 1 \right]}{k^{2} R_{L}}$$
(A.9)

where R_L is the equivalent load impedance of the secondary and k is the coupling coefficient between the primary and secondary. The L_1 can be calculated as 174 pH based on the simulation k value (0.72) from momentum simulator. Therefore, the judicious and optimal design of transformer can provide impedance matching and band-pass filtering to achieve good signal integrity and reject an unwanted baseband signal.

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REFERENCES

- B. Leibowitz *et al.*, "A 4.3 GB/s mobile memory interface with powerefficient bandwidth scaling," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 889–898, Apr. 2010.
- [2] K.-I. Oh et al., "A 5-Gb/s/pin transceiver for DDR memory interface with a crosstalk suppression scheme," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2222–2232, Aug. 2009.
- [3] T.-Y. Oh *et al.*, "A 7 Gb/s/pin GDDR5 SDRAM with 2.5 ns bank-tobank active time and no bank-group restriction," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 434–435.
- [4] J. Poulton, R. Palmer, A. M. Fuller, T. Greer, J. Eyles, W. J. Dally, and M. Horowitz, "A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2745–2757, Dec. 2007.
- [5] K.-L. Wong, H. Hatamkhani, M. Mansuri, and C.-K. Yang, "A 27-mW 3.6-Gb/s I/O transceiver," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 602–612, Apr. 2004.
- [6] M.-J. E. Lee, W. Dally, and P. Chiang, "Low-power area-efficient high-speed I/O circuit techniques," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1591–1599, Nov. 2000.
- [7] K. Fukuda et al., "A 12.3 mW 12.5 Gb/s complete transceiver in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 368–369.
- [8] G.-S. Byun et al., "A 8.4 Gb/s 2.5 pJ/b mobile memory I/O interface using simultaneous bidirectional dual (Base+RF) band signaling," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 488–489.
- [9] H. Wilson and M. Haycock, "A six-port 30 GB/s nonblocking router component using point-to-point simultaneous bidirectional signaling for high-bandwidth interconnects," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1954–1963, Dec. 2001.
- [10] R. Mooney, C. Dike, and S. Borkar, "A 900 Mb/s bidirectional signaling scheme," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1538–1543, Dec. 1995.
- [11] J.-K. Kim et al., "A 3.6 Gb/s/pin simultaneous bidirectional (SBD) I/O interface for high-speed DRAM," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 414–415.
- [12] C. Yoo, K. Kyung, K. Lim, H. Lee, J. Chai, N. Heo, D. Lee, and C. Kim, "A 1.8-V 700-Mb/s/pin 512-Mb DDR-II SDRAM with on-die termination and off-chip driver calibration," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 941–951, Jun. 2004.

- [13] Rogers RO4003, Petlas [Online]. Available: http://www.petlas.fi/ ro4003.htm
- [14] "Advanced Design System User's Guide," Agilent Technology, Palo Alto, CA, 1999.
- [15] K.-S. Ha et al., "A 6 Gb/s/pin pseudo-differential signaling using common-mode noise rejection techniques without reference signal for DRAM interfaces," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 138–139.
- [16] G. Zhang et al., "A BiCMOS 10 Gb/s adaptive cable equalizer," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2132–2140, Nov. 2005.
- [17] M. F. Chang et al., "RF/wireless interconnect for inter- and intra-chip communications," Proc. IEEE, vol. 89, no. 4, pp. 456–466, Apr. 2001.



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