SAI-WANG (ROCCO) TAM

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EDUCATION:

Ph.D. in Electrical Engineering June 2009
UNIVERSITY OF CALIFORNIA, LOS ANGELES
Major Field: Integrated Circuit and Systems
Minor Fields: Communication, Photonics
Dissertation: "RF-Interconnect for Future Network-on-Chip"
Advisor: Professor M-C. Frank. Chang
Published 17 conference papers/Journals (4 additional papers in preparation), 1 Book Chapter and 5 patents pending

Master of Science in Electrical Engineering June 2008
UNIVERSITY OF CALIFORNIA, LOS ANGELES

Bachelor of Science in Electrical Engineering with Honor June 2003
UNIVERSITY OF CALIFORNIA, LOS ANGELES

RESEARCH INTERESTS

- (10GHz to 1THz) mm/sub-mm/THz circuits and system especially in RF/Wireless interconnects, multi-band frequency oscillator and imaging system
- Network-On-Chip and ultra-high performance computer architecture
- High speed analog mixed-signal circuits
- Ultra-low power wireless circuits and system

HONORS AND AWARDS

2010 IEEE RFIC Sym, May. 2010, Top 10 Finalist on Best Paper Award
2009 GRC/FCRP/NRI Inventor Recognition Award
2008 IEEE HPCA Sym, Feb. 2008, Best Paper Award
2001 US Department of Energy, Undergraduate Research Fellowship

RESEARCH EXPERIENCE

6/09 – 5/10 *Postdoctoral Scholar* – Department of Electrical Engineering, UCLA
9/04 – 6/09 *Research Assistant* – Department of Electrical Engineering, UCLA
1/04 – 6/04 *Teaching Assistant* – Department of Electrical Engineering, UCLA
5/01 – 9/01 *Undergraduate Research Fellow* – Lawrence Berkeley National Laboratory

INDUSTRIAL EXPERIENCE

08/11–Present *Senior RFIC Design Engineer* – Marvell Semiconductor, Inc, Santa Clara, CA
06/10 – 07/11 *Senior RFIC Architect* – TagArray, Inc, Palo Alto, CA
10/08 – 05/10 *Founding Member, Principal RFIC Design Engineer* – WaveConnex, Inc, Los Angeles, CA
06/06 – 09/06 *Analog Mixed Signal Circuit Design Intern* – Intel Corp, Santa Clara, CA
06/05 – 12/05 *Analog Mixed Signal Circuit Design Intern* – Intel Corp, Hillsboro, OR

INDUSTRIAL EXPERIENCE HIGHLIGHTS

Rocco has extensive industry experience in both early stage start-ups and well established companies.

Experience in early stage start-ups:

Founder Member, Principal RFIC Design Engineer, Oct 2008-May 2010
WaveConnex, Inc, Los Angeles, CA

- Invented the innovative ultra-short distance 60GHz wireless interconnect technology
    - The inventor of the company's first three Patents
- Lead both research and product development at the early stage
    - Successfully developed and demonstrated the first proof of concept prototype in 65nm CMOS process which includes 60GHz transceiver (VCO,PA, LNA and BaseBand), antenna and PCB.
    - Responsible for all the design in mm-wave CMOS RFIC, on-chip antenna, high speed PCB and mm-wave testing
    - The first prototype achieved 20X better performance than any other existing competitor product
    - Designed the first product prototype for customer evaluation
    - Currently the first generation product is shipping at 1M units pre-month
- Responsible for the strategic technology road-map in transceiver architecture, mm-wave circuit and antenna
    - Key Contributor to the investor presentation and proposal
    - Resulting total $ 7M VC funding for the company

RFIC Architect, Jun 2010 – Aug 2011
TagArray, Inc, Palo Alto, CA

- Technical lead of a small team on the next generation ultra-low power UWB transceiver for RFID
- Responsible for all the design from system level architecture to circuit implementation
    - Sub-micro-Watt circuit and system design
    - RFID Reader design including LNA, Mixer, VCO and PLL
    - Successfully demonstrated the first prototype

Experience in well established companies:

Senior RFIC Design Engineer, Aug 2011 - Present
Marvell Semiconductor, Inc, Santa Clara, CA

- WiFi transceiver 4X4 MIMO SoC circuits design
- On-chip CMOS power amplifier design in both 40nm and 28nm CMOS technology
- Part of the team to design and evaluate the digital pre-distortion for the power amplifier
- Preliminary studies on the latest CMOS 60GHz transceiver SoC project

Co-op Analog Mixed Signal Circuit Design Engineer
Intel Corporation, Santa Clara, CA and Portland, OR
Jun 2006 – Sep 2006, Jun 2005 – Dec 2005, Mar 2004 – Sep 2004

- Designed voltage regulator for power management system in multi-core processors
- Worked in a group which was responsible for preliminary analog scaling design in 32nm process
- Implemented various large scale transistor level (order of +100,000 devices) mixed-signal circuit system model in the latest multi-core microprocessor in 65/45nm CMOS technology
- Responsible for developing mixed-signal Verilog AMS model for multiple PLLs and DLL clocking generation
- Designed and verified high speed I/O data path circuits such as sense amplifier and internal reference generator and performed various layout planning with layout engineer
- Developed and simulated a transistor level I/O buffer timing model which can estimate one of the most critical product specification parameter of the latest Pentium Processor project

RESEARCH HIGHLIGHTS

RF-Interconnect For Future Network-On-Chip (Ph.D. Dissertation Topic)

On-chip interconnects have been projected as the limiter in nanometer designs in terms of power and latency. The communication infrastructure would significantly impact the performance, area, and power of future network-on-chips (NoCs). To mitigate this impact on future for NoCs, we explored the use of RF-interconnect (RF-I) over on-chip transmission lines that can simultaneously communicate among multiple communication channels with reconfigurable bandwidth allocation, and yet provide low energy per bit.

Major Contributions:

- Demonstrated the first 10Gb/s tri-band (30GHz, 50GHz + BaseBand) on-chip RF-Interconnect for future NoC (VLSI 2009[7], 1 Book Chapter [15], both first author), 2 Tape-outs in IBM 90nm
- Developed a RF-Interconnect scaling model for future NoC for computer architect simulator which resulted 5 top computer architecture conference papers [14-20, co-author] and one best paper award(HPCA 2008, acceptance rates <10%). Since our team was comprised of 5 students and 3 professors, the authors are listed in alphabetical order in all 5 papers.
- One of the main contributors on a funding proposal which amounted to $10M dollars granted by NSF to establish a new multi-discipline Customizable Domain-Specific Computing Research Center

Multi-Band mm-Wave Oscillator

This work presented three techniques, sub-harmonic injection locking, left-handed (LH) and even-odd mode , which are suited to mm-wave multiband applications.

Major Contributions:

- Developed three multi-band oscillator techniques in mm-wave frequencies
- Sub-harmonic injection locking (20GHz & 60GHz) mm-wave oscillator (RFIC 2008[12], first author)
- Dual Band (20GHz and 55GHz) left-handed mm-wave oscillator with largest 35GHz band selection range (RFIC 2009[11], first author + 1 Journal [10], second author with equally contribution as the first author.)
- The first Quad-band (43GHz, 48GHz, 57GHz, 74GHz) mm-wave oscillator (RFIC 2010[9], second author with equally contribution as the first author.)
- Mentored 1 Ph.D. student for 4 years, 3 Tape-outs (1 in IBM 90nm, 2 in TSMC 65nm)

RF-Interconnect For Advance Memory Interface

In this work, we explore the use of RF-interconnect (RF-I) over an off-chip transmission line that can simultaneously communicate among multi-core CPUs and DRAMs with reconfigurable bandwidth allocation, and provide much lower energy per bit.

Major Contributions:

- Leader and mentor of a small research team (2 Ph.D Students +1MS student) for 4 years, 2 Tape-outs
- Co-developed the RF-Interconnect system architecture and circuits for advance memory interface
- 1 Co-author paper (ISSCC 2011[2]), 1 patent and 1 Journal paper (JSSC [3])

Short-Range mm-Wave Wireless RF-Interconnect

Connectivity becomes the ultimate limitation in many consumer electronics due to bulky connectors between different layers of a printed circuit board. A new technique using wireless RF interconnect (WRF-I) with asynchronous modulation scheme is utilized for ultra short distance (less than 10cm) chip to chip or board to board multi-gigabit communication with higher data rate and better mechanical reliability

Major Contribution:

- Solely demonstrated and developed the first ultra-short distance mm-wave (60GHz) wireless communication system (~10Gbps) in 65nm CMOS process which resulted a $7M VC funding for a

semi-conductor startup, WaveConnex. (3 patents pending, 2 Journals submitted, 2 invited conference workshop papers [4-5])

Other Research Projects

Digital Controlled Artificial Dielectric (DiCAD) (MTTS 2008 [10], second author with equally contribution as the first author) can digitally control the effective dielectric constant of a differential mode transmission line up to 60GHz in 90nm CMOS
Major Contribution: wafer-scale mm-wave measurement and on-chip transmission line design
10Bit 1 GSample/s Folding ADC (BCTM 2008[15], second author)
Major contribution: designed 1GSample distributed T&H, comparator and digital logic in 0.35µm BiCMOS

PUBLICATIONS

RF/Wireless-Interconnect:

1. **Sai-Wang Tam**, Yanghyo Kim, M.-C. F Chang, "*Periodic Near Field Directors (PNFD*) for *Multi Gbps Milli-Meter-Wave high voltage isolator," to be submitted to* IEEE Microwave and Wireless Components Letter, (75% done)
2. **Sai-Wang Tam**, Yanghyo Kim, M.-C. F Chang, "*A Multi Gbps Short-range Milli-Meter-Wave-Wireless-Interconnect (M2W2-Interconnect)*," submitted to IEEE J. of Solid-State Circuits
3. Gyung-Su Byun, Yanghyo Kim, Jongsun Kim, **Sai-Wang Tam**, M-C. F Chang, "*An Energy-Efficient and High-Speed Mobile Memory I/O Interface Using Simultaneous Bi-Directional Dual (Base+RF)-Band Signaling*,", Jan 2012, IEEE J. of Solid-State Circuits
4. **Sai-Wang Tam**, Jongsun Kim, M-C. F Chang , "The next generation RF/Wireless-interconnect," special session Wireless Raplacement of Wireline I/Os in IEEE RFIT Symposium, 2011, Invited Workshop paper
5. **Sai-Wang Tam**, Jongsun Kim, M-C. F Chang , "The next generation RF/Wireless-interconnect," special session on Architectures and Circuits for Next-Generation High-Speed Interfaces, the 5^{4th} IEEE International Midwest Symposium on Circuit and Systems, 2011, Invited Workshop paper
6. Gyung-Su Byun, Yanghyo Kim, Jongsun Kim, **Sai-Wang Tam**, Jason Cong, Glenn Reinman, M-C. F Chang, "*An 8.4Gb/s 2.5pJ/b Mobile Memory I/O Interface Using Bi-directional and Simultaneous Dual (Base+RF)-Band Signaling*," IEEE International Solid-State Circuits Conference (ISSCC 2011)
7. **Sai-Wang Tam**, Eran Socher, Alden Wong, M.-C. F. Chang, *"A simultaneous tri-band on-chip RF-interconnect for future network-on-chip,"* VLSI Circuits, 2009 Symposium on , vol., no., pp.90-91, 16-18 June 2009

Multi-Band mm-Wave CMOS Oscillator:

8. **Sai-Wang Tam**, Yanghyo Kim, A.H-T Yu, D. Murphy, Tim LaRocca, Daquan Huang, M.-C. F Chang, T. Itoh, " Techniques on wide tuning range and multi-band CMOS oscillator in mm-wave frequencies," a review Journal to be submitted to Special issues on Microwave Theory and Techniques, IEEE Transactions, (50% done)
9. A.H-T Yu, **Sai-Wang Tam**, D. Murphy, M.-C.F Chang, T. Itoh, *"A mm-Wave Arbitrary 2^N Band Oscillator Based on Even-Odd Mode Technique,"* Radio Frequency Integrated Circuits Symposium, 2010. RFIC 2010.May 2010

10. A.H.-T. Yu, **Sai-Wang Tam**, Yanghyo Kim, Eran Socher, W Hant, M.-C.F. Chang, T Itoh, *"A Dual-Band Millimeter-Wave CMOS Oscillator With Left-Handed Resonator,"* Microwave Theory and Techniques, IEEE Transactions on , vol.58, no.5, pp.1401-1409, May 2010

11. **Sai-Wang Tam**, A.H-T. Yu, Yanghyo Kim, E Socher, M.C.F Chang, T. Itoh, *"A dual band mm-wave CMOS oscillator with left-handed resonator,"* Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE , vol., no., pp.477-480, 7-9 June 2009

12. **Sai-Wang Tam**, Eran Socher, Alden Wong, Yu Wang, Lan Duy Vu, M.-C. Frank Chang, "*Simultaneous Sub-harmonic Injection-Locked mm-Wave Frequency Generators for Multi-band Communications in CMOS,"* 2008. RFIC 2008. IEEE , vol., no., pp.131-134, June 17 2008-April 17 2008

13. Tim LaRocca, **Sai-Wang Tam**, Daquan Huang, Qun Gu, Eran Socher, William Hant, Frank Chang, "*Millimeter-Wave CMOS Digital Controlled Artificial Dielectric Differential Mode Transmission Lines for Reconfigurable ICs,"* IEEE International Microwave Symposium (IMS'08).

Computer Architecture:

14. **Sai-Wang Tam**, Mishali Naik, Eran Socher, Glenn Reinman, Jason Cong, M.-C. F Chang, "Circuits and architecture in scalable network-on-chip using o*n-chip RF-interconnect,"* to be submitted to Transaction on VLSI

15. **Sai-Wang Tam**, M.-C. Chang, J. Cong, G. Reinman, E. Socher, *"RF-Interconnect for future network-on-chip,"* Low Power Network-on-Chip, (Book Chapter 10), Springer, First Edition 2010

16. Suk-Bok Lee, **Sai-Wang Tam**, Ioannis Pefkianakis, Songwu Lu, M. Frank Chang, Chuanxiong Guo, Glenn Reinman, Chunyi Peng, Mishali Naik, Lixia Zhang, Jason Cong, *"A Scalable Micro Wireless Interconnect Structure for CMPs"*, ACM MOBICOM 2009, pp.217-228, 20-25 September 2009

17. J. Cong, M.-C.F. Chang, G. Reinman, **Sai-Wang Tam**, *"Multiband RF-Interconnect for Reconfigurable Network-on-Chip Communications,"* System Level Interconnect Prediction (SLIP 2009), pp.107-108, July 2009,(alphabetical order)

18. Chang M-CF, Cong J, Kaplan A, Chunyue Liu, Naik M, Premkumar J, Reinman G, Socher E, **Sai-Wang Tam**, *"Power reduction of CMP communication networks via RF-interconnects,"* 2008 41st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-41). pp. 376-87, Lake Como, Italy. 8-12 Nov. 2008, (alphabetical order)

19. M. Frank Chang, Jason Cong, Adam Kaplan, Mishali Naik, Glenn Reinman, Eran Socher, **Sai-Wang Tam**, *"CMP Network-on-Chip Overlaid With Multi-Band RF-Interconnect,"* High Performance Computer Architecture, 2008. HPCA 2008. IEEE 14th International Symposium on , vol., no., pp.191-202, 16-20 Feb. 2008,(alphabetical order), **Best Paper Award**

20. M. Frank Chang, Eran Socher, **Sai-Wang Tam**, Jason Cong, and Glenn Reinman. *"RF Interconnects for Communications On-Chip*," International Symposium on Physical Design (ISPD), Apr 2008

High-Speed Mixed-Signal Circuit Design

21. A Razzaghi. **Sai-Wang Tam**, P. Kalkhoran, Yu Wang, Chih-Yi Kuan, B Nissim, Lan Duy Vu. Chang MCF, *"A single-channel 10b 1 GS/s ADC with 1-cycle latency using pipelined cascaded folding"*, 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM. Monterey, CA, USA. 13-15 Oct. 2008

22. Sandeep D'Souza, **Sai-Wang Tam**, Adrian Tang, M.-C. Frank Chang, A 2GS/s 10-bit DAC-DDFS-based IQ Modulator for a Self-Healing 60GHz Wireless Transceiver, submitted to Radio Frequency Integrated Circuits Symposium, 2012

PATENTS

23. *On-chip Radio Frequency (RF) Interconnects for Network-On-Chip Designs,* Patent application 12/363,182 (pending)
24. *MM-wave-Wireless-Interconnect Method for Short-Range communication with ultra-high Data Rate Capability,* Patent Application 61/185,946 (pending)
25. *Off-chip Multi-band RF-Interconnect (OMRF-I) Transceiver for Future Advanced High Speed Memory Interface,* (pending)
26. *Periodic Near Field Directors (PNFD) for Short-range Milli-Meter-Wave-Wireless-Interconnect (M2W2-Interconnect),* (pending)
27. *Arbitrary 2^N band oscillator based on even-odd mode technique at mm-wave frequencies,* (pending)

Talks and Seminars

28. *"RF/Wireless Interconnect, The Next Wave of Connectivity,"* Invited Talk, University of California, Davis, USA, May 2011
29. *"RF/Wireless Interconnect, The Next Wave of Connectivity,"* Invited Talk, Hong Kong University of Science and Technology, Hong Kong SAR, PRC, Feb 2011
30. *"RF/Wireless Interconnect, The Next Wave of Connectivity,"* Invited Talk, City University of Hong Kong, Hong Kong SAR, PRC, Sept 2010
31. *"Research overview on RF-Interconnect for NoC,"* Annual Research Review, NSF Center for Domain Specific Computing, UCLA, Los Angeles, USA, June 2010
32. *"RF-Interconnect for future NoC,"* Invited Talk, RamBus, Mountain View, USA, Feb 2010
33. *"RF-Interconnect for future NoC,"* Research Seminar, Kyoto University, Kyoto, Japan, June 2009
34. "*A simultaneous tri-band on-chip RF-interconnect for future network-on-chip,"* VLSI Circuits, 2009 Symposium, Kyoto, Japan, June 2009
35. *"A Dual-Band Millimeter-Wave CMOS Oscillator With Left-Handed Resonator,"* Radio Frequency Integrated Circuits Symposium, 2009, Boston, USA, June 2009
36. *"RF-Interconnect for future NoC,"* Ph.D. Final Defense, UCLA, Los Angeles, USA, May 2009
37. *"Research overview on RF-Interconnect and mm-wave CMOS,"* DARPA Annual TAPO Design review, Vermont, USA, Sept 2008
38. *"Simultaneous Sub-harmonic Injection-Locked mm-Wave Frequency Generators for Multi-band Communications in CMOS,"* Radio Frequency Integrated Circuits Symposium, 2008, Atlanta, USA, June 2008

RESEARCH MENTORSHIP EXPERIENCE

As a senior Ph.D. student and postdoctoral scholar, I have successfully mentored 2 Ph.D. students and 4 M.S. students through their gradation.

1. Alvin Hsing-Ting Yu, *"Multi-Frequency Generation in CMOS for mm-Wave System Application,"* Ph.D. Spring 2010
    - Mentored from 2006 to 2010
    - Introduced him the basic RFIC design technique from on-chip passive element all the way to full chip simulation and testing
    - Co-developed multi-band frequency oscillator technique with largest tuning range

- Co-authored several proposals and research reports to the funding agency
- Co-worked with him for 2 Tape-out in TSMC 65nm CMOS
- Hosted daily one-on-one meeting in the first 2 years and weekly meeting in next 2 years

2. Gyungsu Byun, *"Multi-band RF-Interconnect for Future Memory Interface,"* Ph.D. Spring 2010
   - Mentored from 2005 to 2010
   - Introduced him the basic RFIC design technique from on-chip passive element all the way to full chip simulation and testing
   - Co-developed the first system and circuits architecture on RF-Interconnector for future memory interface
   - Co-authored several proposals and research reports to the funding agency
   - Co-worked with him for 3 Tape-out in TSMC 65nm CMOS and UMC 90nm CMOS
   - Hosted daily one-on-one meeting in the first year and weekly meeting in next 3 years
3. Rod Kim, *"A 20GHz RF transceiver for RF-Interconnect,"* M.S. Spring 2010, (mentored since 2008)
4. Sunny Sharma. "*A Reconfigurable Low Drop-out Regulator in 65nm CMOS technology,"* M.S. Spring 2010, (mentored since 2008)
5. Lan Vu, *"A 20GHz PLL for on-Chip RF-Interconnect in 90nm CMOS technology,"* M.S. Spring 2006 (mentored from 2004 to 2006)
6. Yu Wang, *"Multi-band frequency generation technique for RF-Interconnect,"* M.S. Spring 2006 (mentored from 2004 to 2006)

TEACHING EXPERIENCE

2005-2006 Teaching Assistant, Basic Analog Electronics Lab, UCLA, EE 110L

PROFESSIONAL ACTIVITIES

2008 – Present	*Reviewer*, IEEE Journal of Solid State Circuits
	Reviewer, IEEE Transaction of VLSI
	Reviewer, IEEE Communication Magazine
	Reviewer, IEEE Microwave and Wireless Components Letters
2009 – Present	*Member*, IEEE
2004 – 2009	*Student Member*, IEEE

WORK STATUS

- U.S. Citizen

References

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Prof. Jason Cong, *Chancellor's Professor of Computer Science, Former Department Chair at UCLA CS Department*
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